FIG. 1

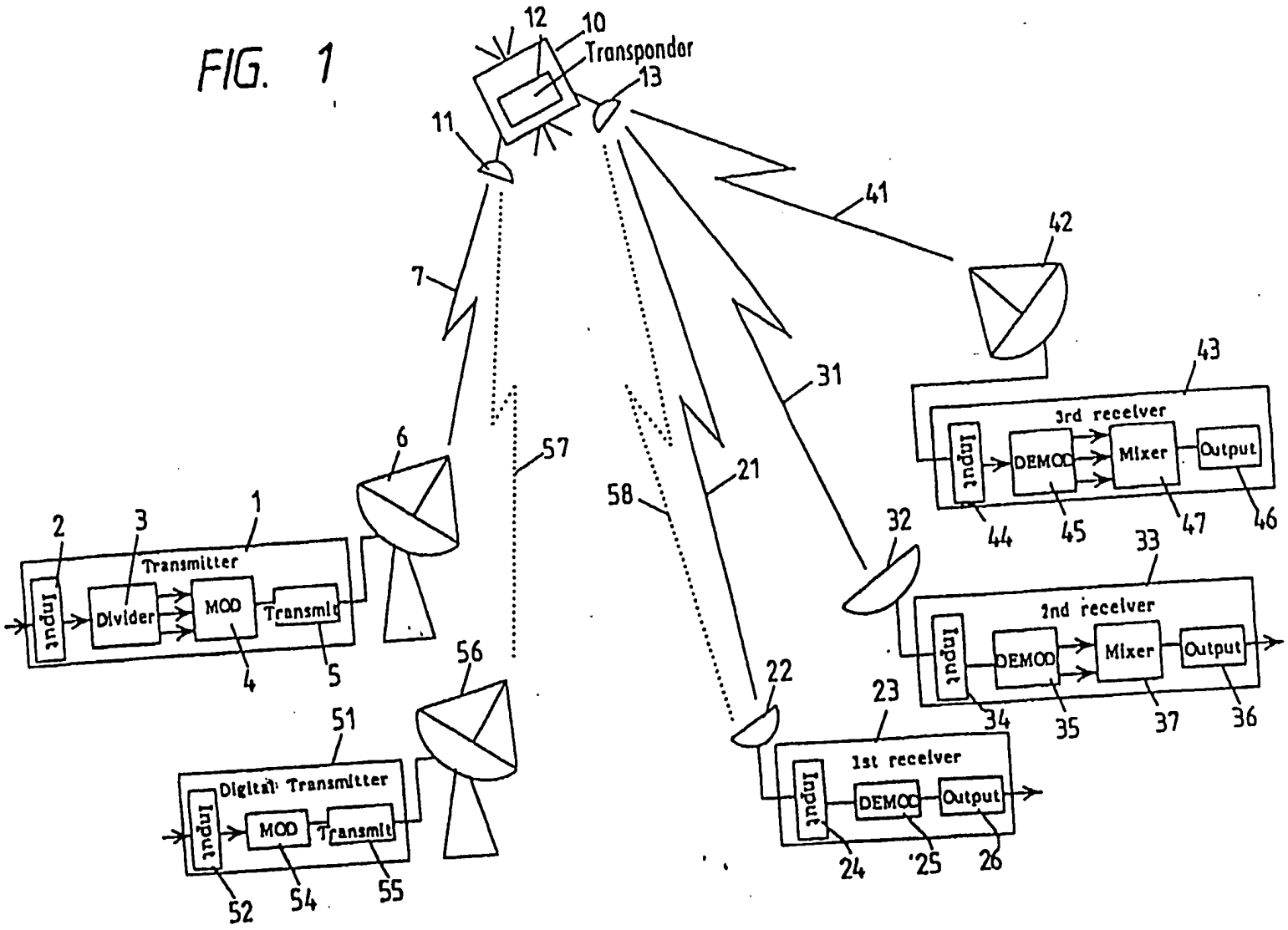

12
10
Transponder
13
11
41
42
7
31
43
3rd receiver
Input
DEMOD
Mixer
Output
44
45
47
46
6
57
21
58
32
33
2nd receiver
Input
DEMOD
Mixer
Output
34
35
37
36
2
3
1
Transmitter
Input
Divider
MOD
Transmit
4
5
56
22
23
51
1st receiver
Input
DEMOD
Output
24
25
26
Digital Transmitter
Input
MOD
Transmit
52
54
55

FIG. 2

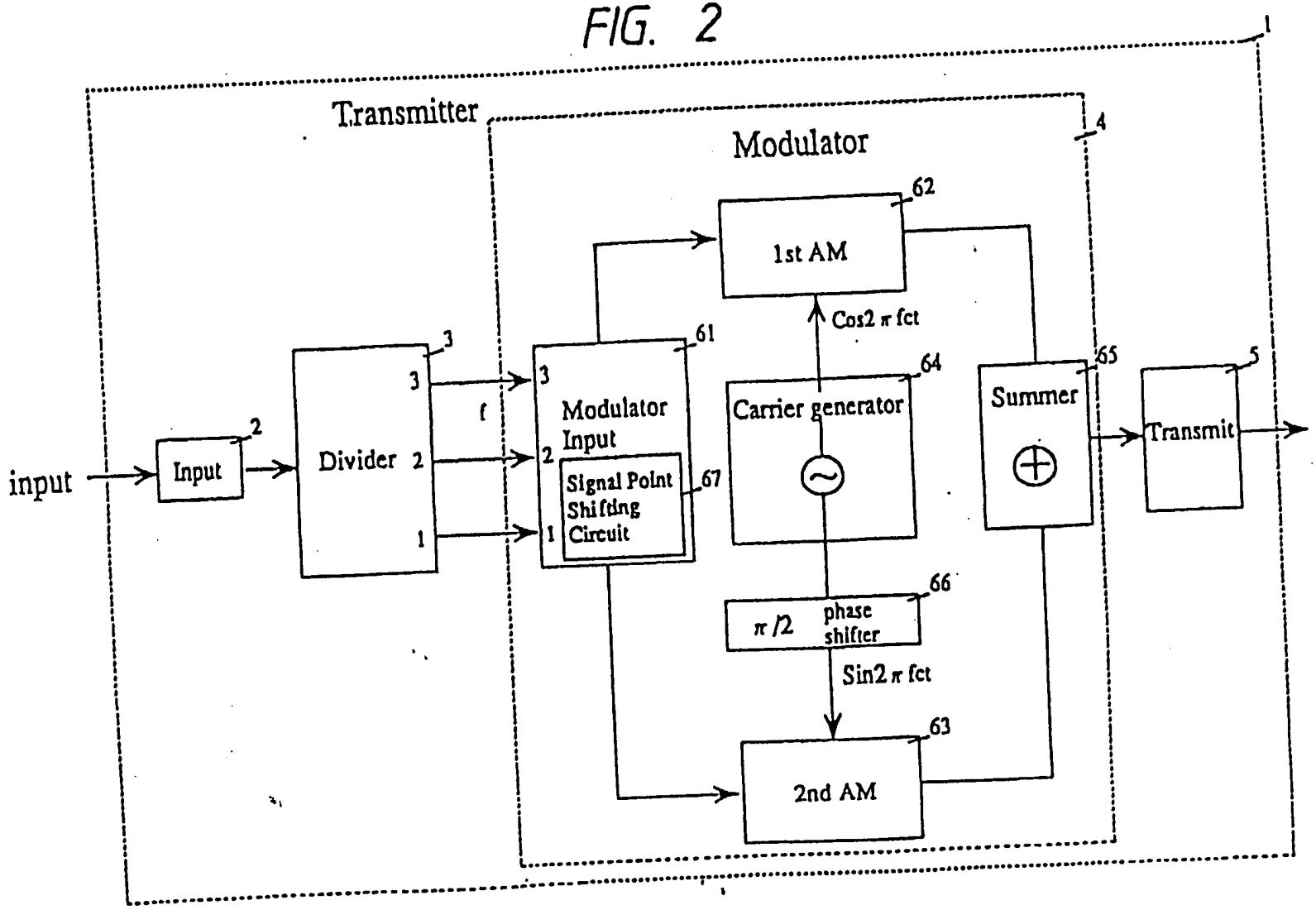

Transmitter
1
Modulator
4
62
1st AM
Cos2 π fct
61
3
Modulator Input
2
Signal Point Shifting Circuit
67
1
3
f
2
1
Divider
3
2
Input
input
64
Carrier generator
65
Summer
5
Transmit
66
π /2 phase shifter
Sin2 π fct
63
2nd AM

FIG. 3

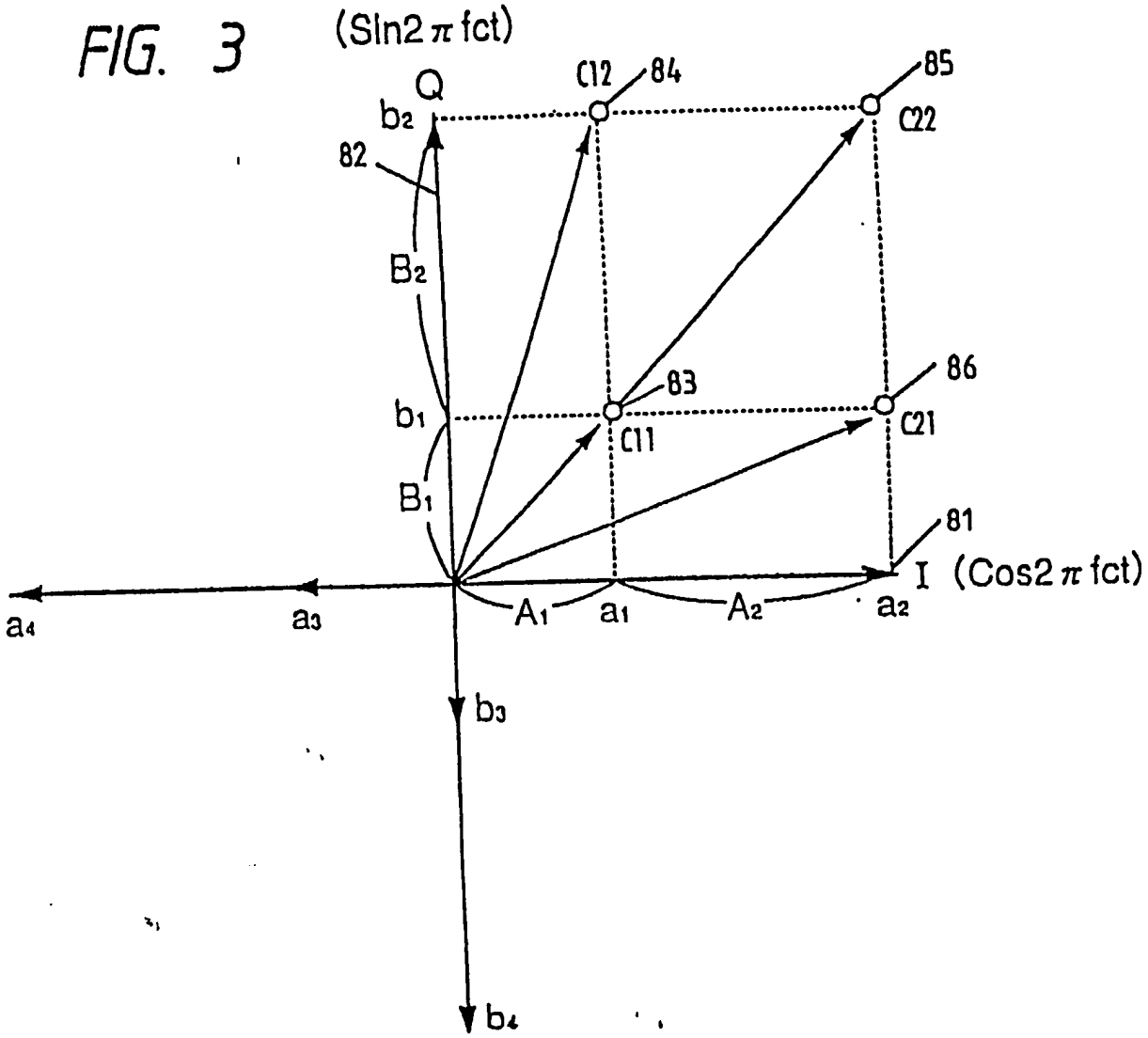

(Sin2πfct)
Q
b2
82
B2
b1
B1
C12
84
85
C22
83
86
C11
C21
81
I
(Cos2πfct)
a4
a3
A1
a1
A2
a2
b3
b4

FIG. 4

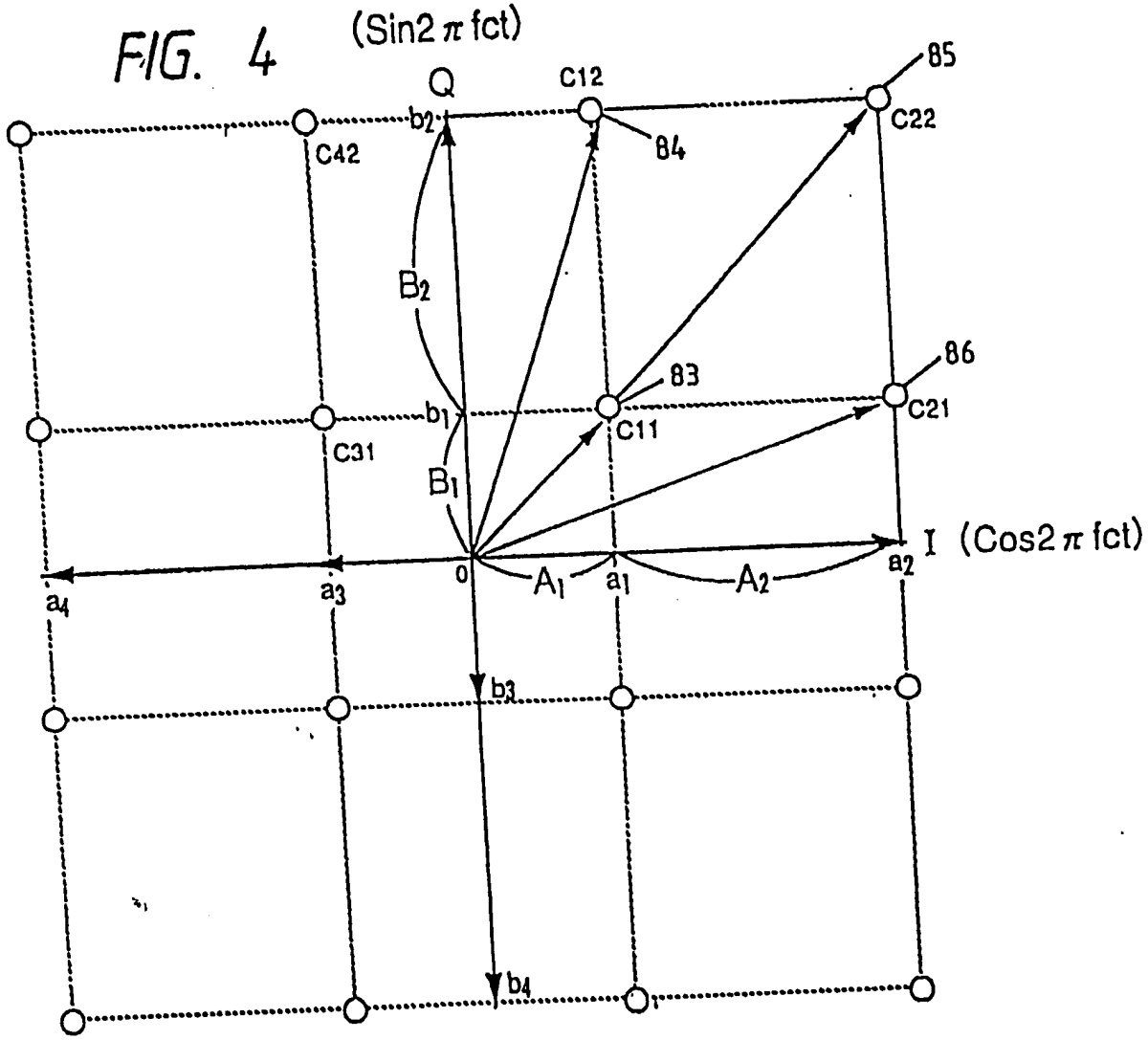

(Sin2 π fct)
Q
C12
85
C22
C42
b2
84
B2
86
83
C21
b1
C11
C31
B1
I (Cos2 π fct)
a4
a3
0
A1
a1
A2
a2
b3
b4

FIG. 5

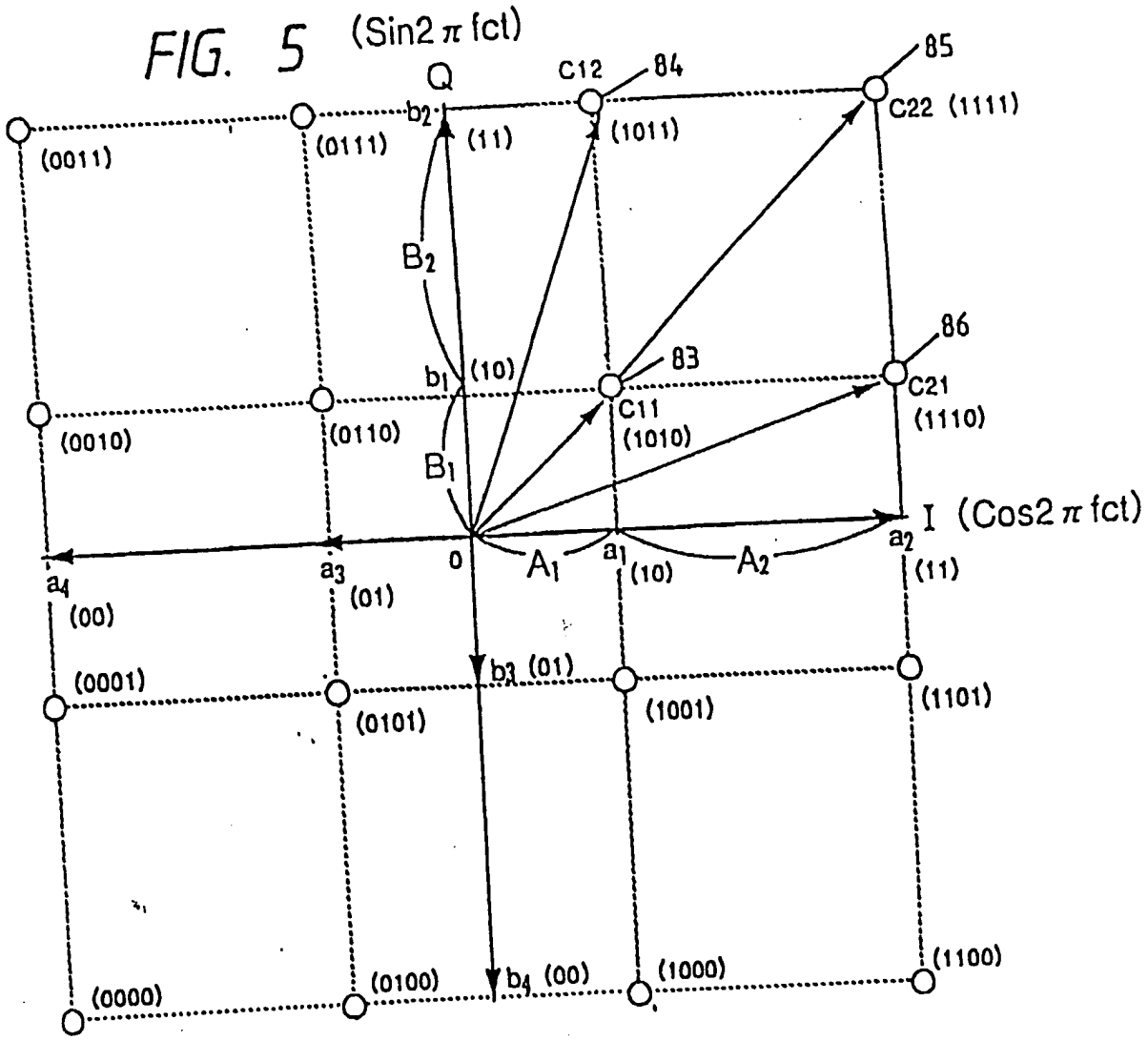

(Sin2 π fct)
Q
C12
84
85
C22 (1111)
b2
(11)
(1011)
(0011)
(0111)
B2
86
83
b1
(10)
C21
(1110)
C11
(1010)
(0010)
(0110)
B1
I (Cos2 π fct)
a2
(11)
a4
(00)
a3
(01)
0
A1
a1
(10)
A2
b3 (01)
(0001)
(0101)
(1001)
(1101)
(0000)
(0100)
b4 (00)
(1000)
(1100)

FIG. 6

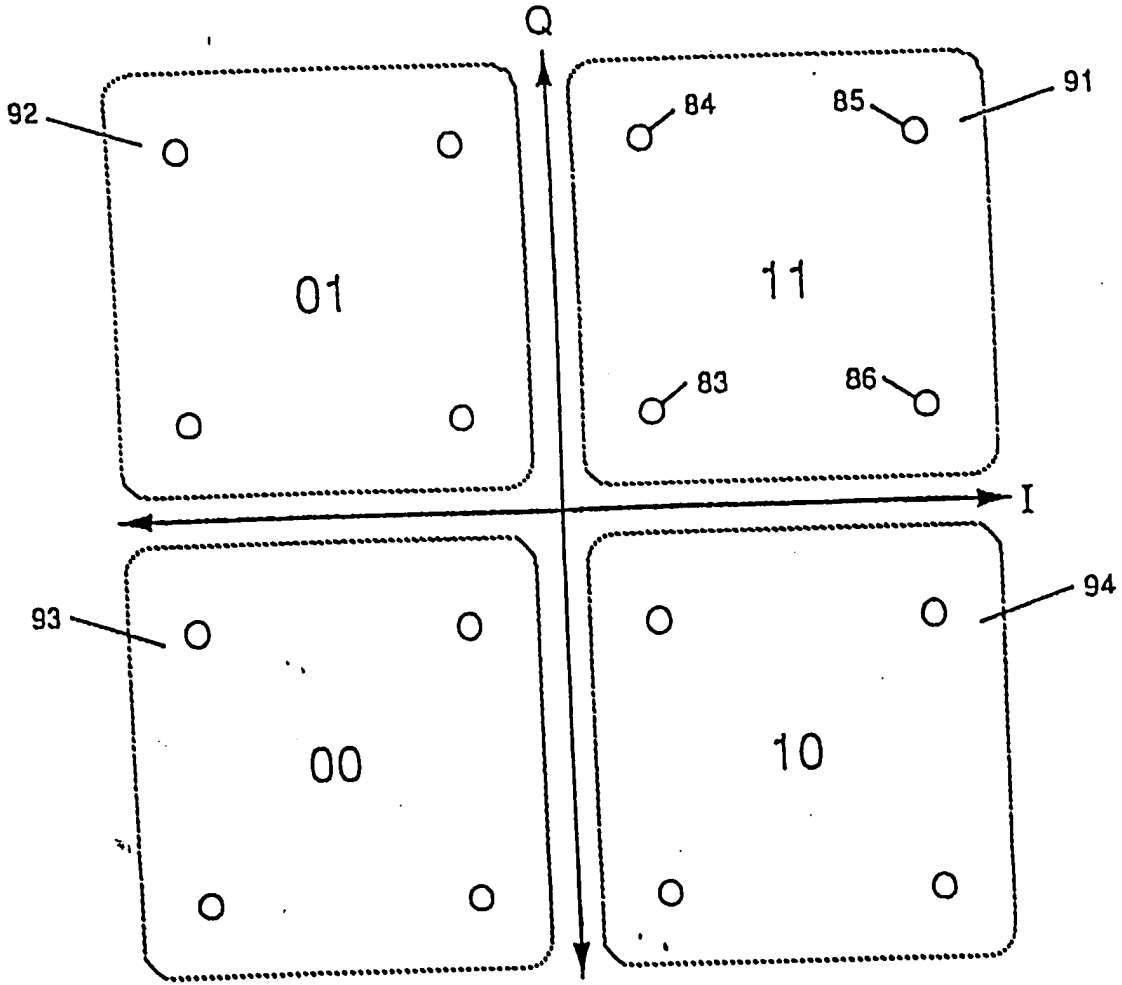


FIG. 7

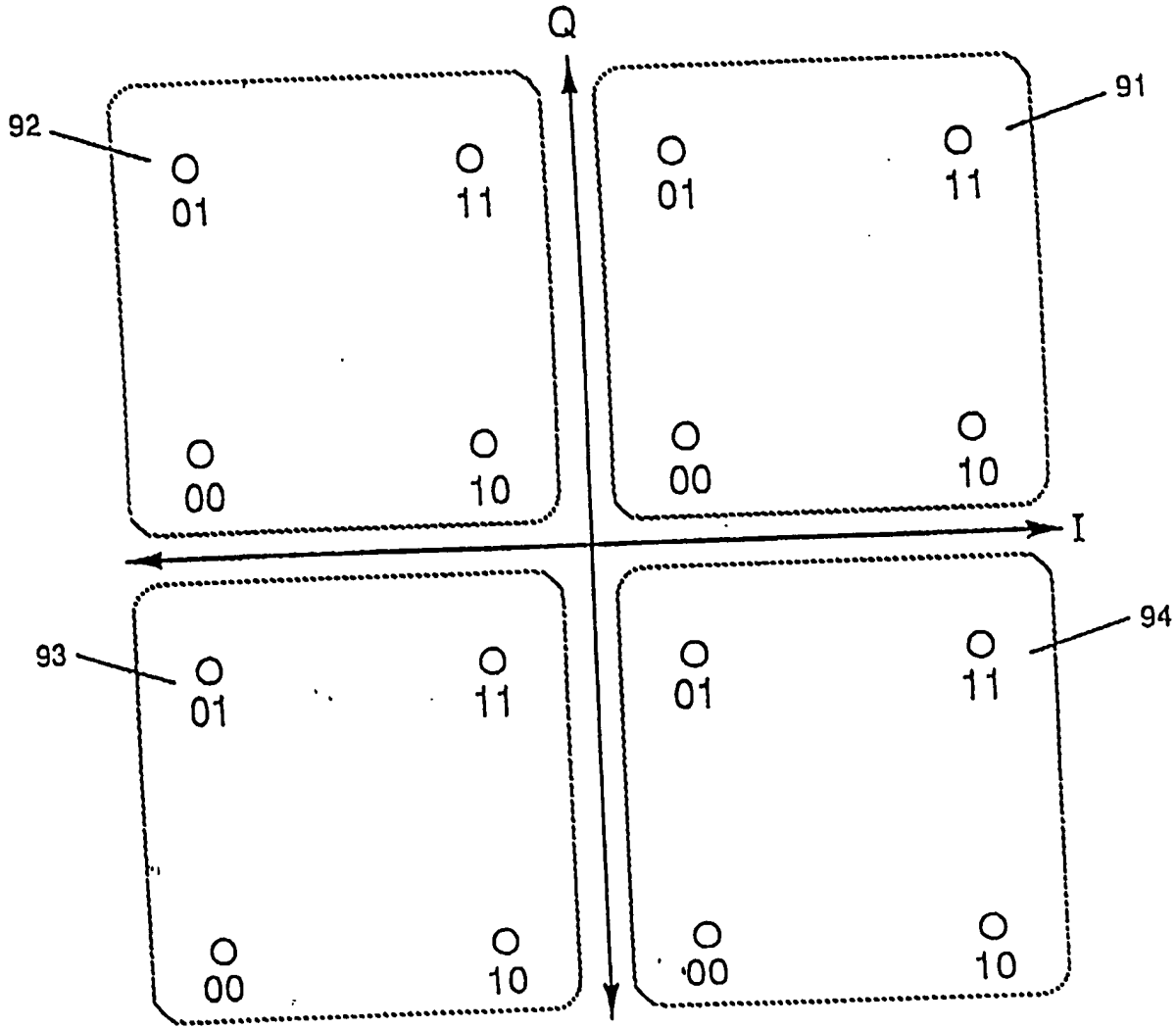


FIG. 8

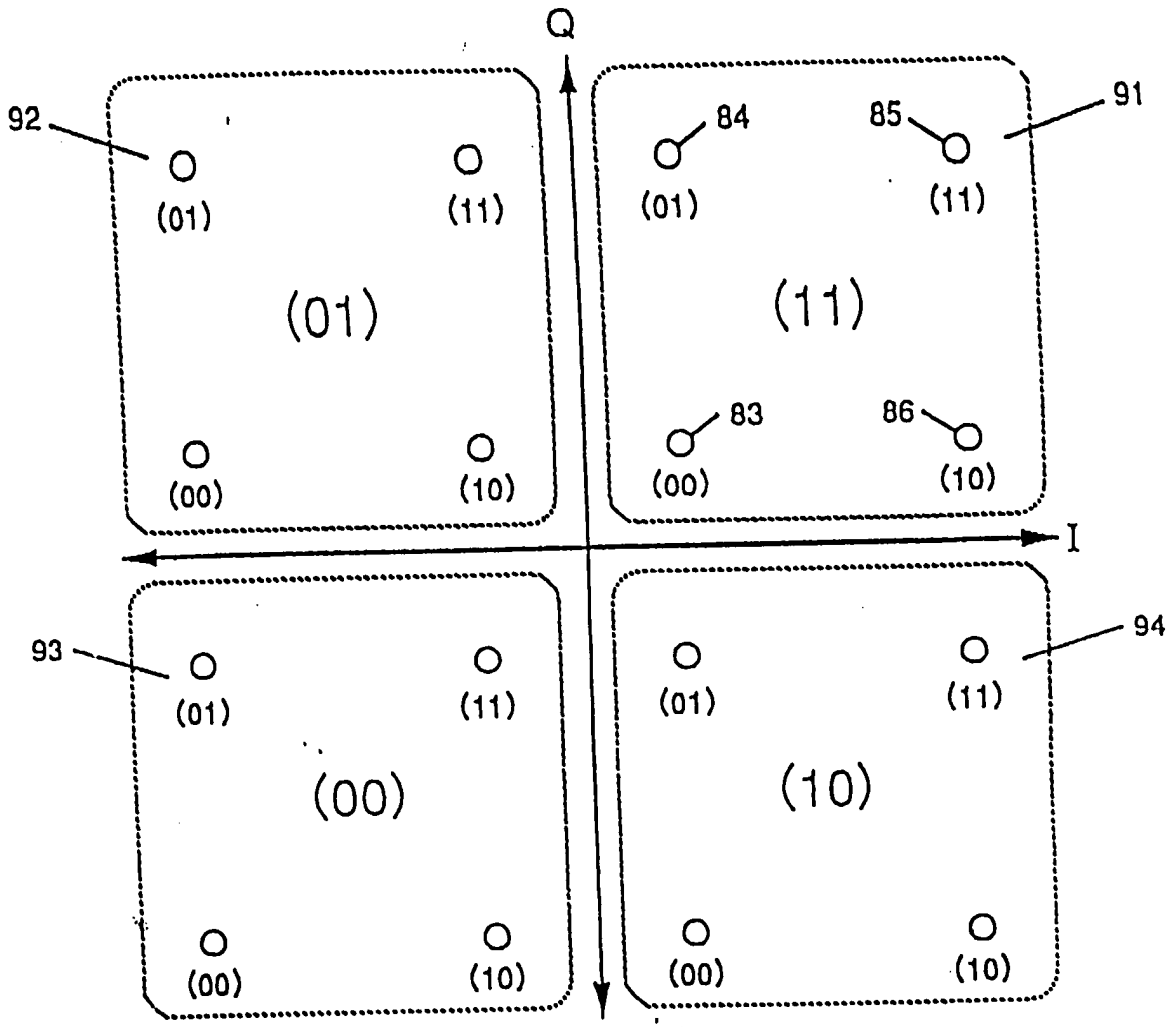

Q
I
92
91
93
94
84
85
83
86
(01)
(11)
(00)
(10)
(01)
(11)
(00)
(10)
(01)
(11)
(00)
(10)
(01)
(11)
(00)
(10)

FIG. 9

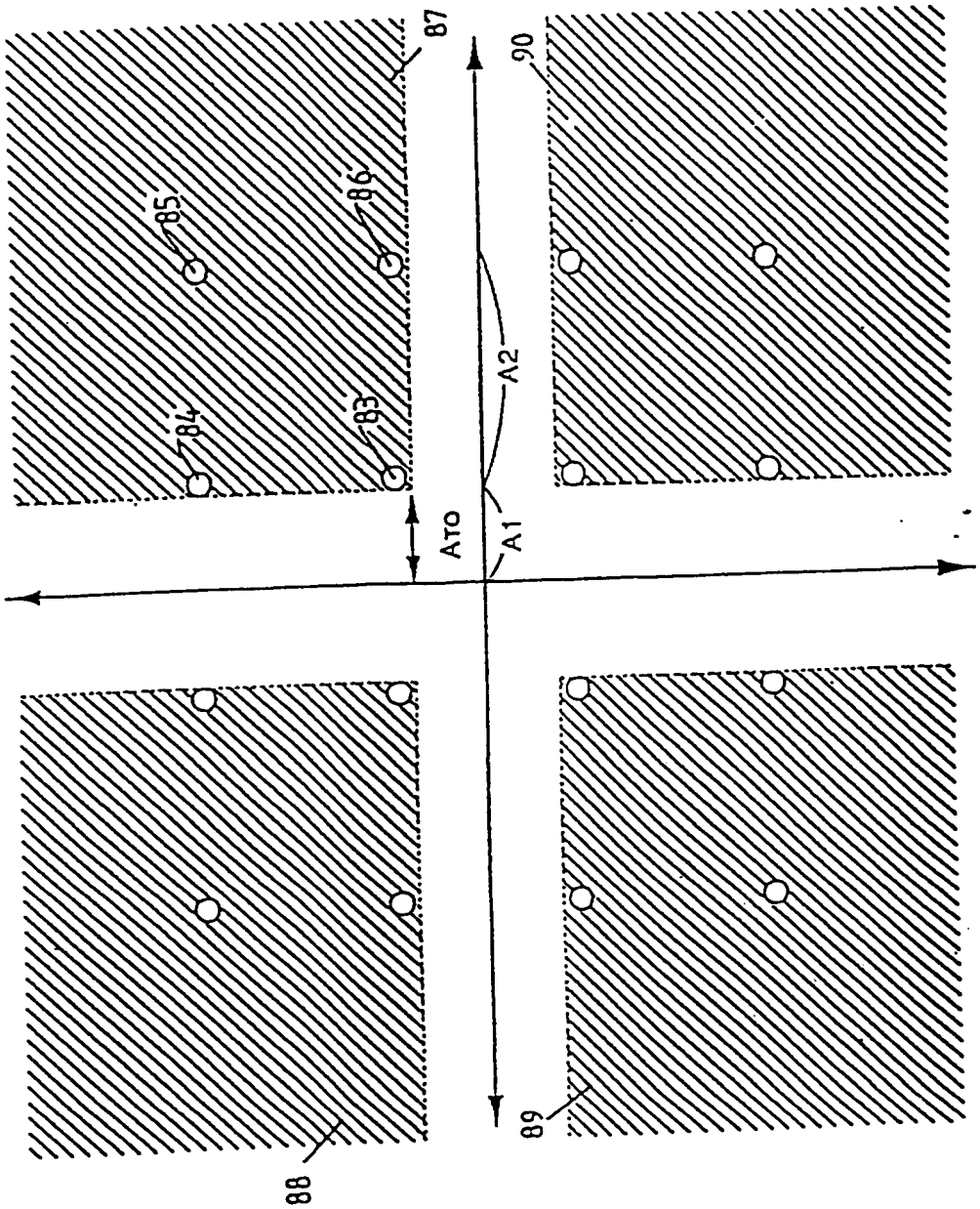


FIG. 10

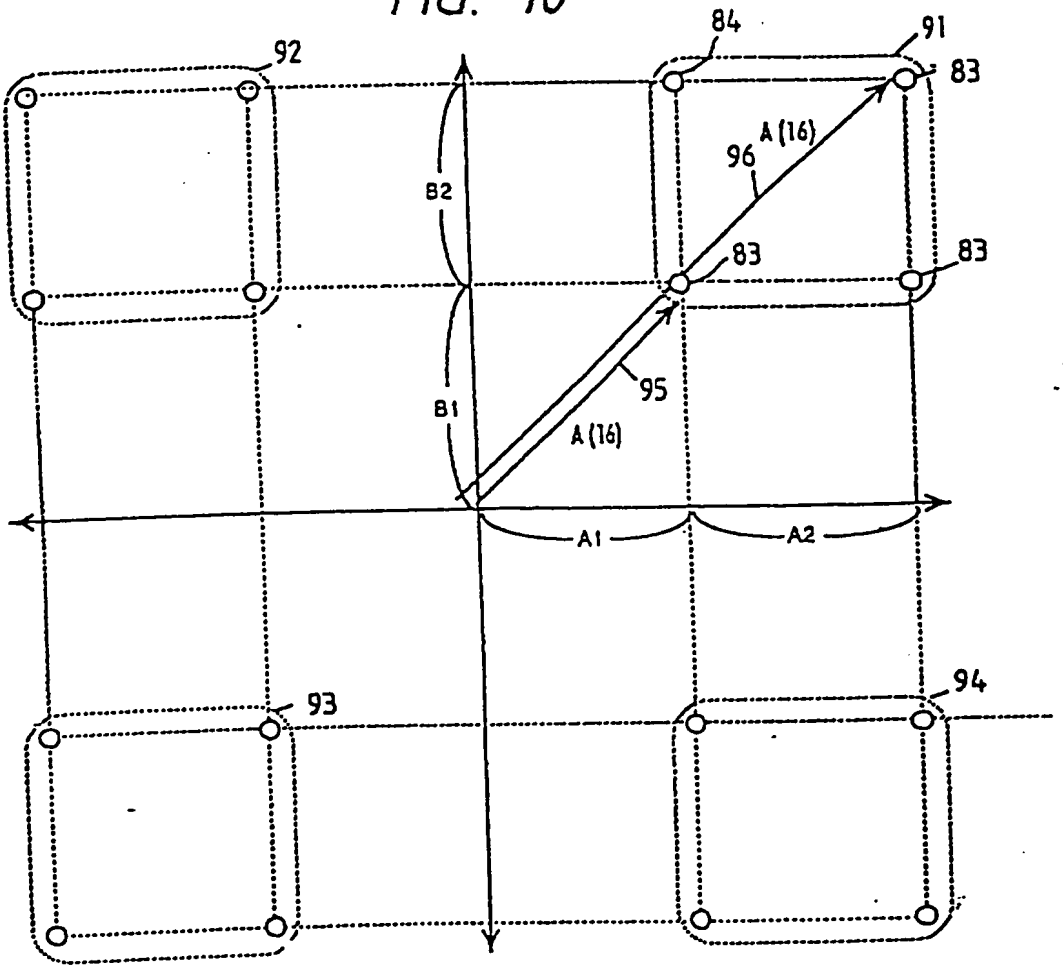


FIG. 11

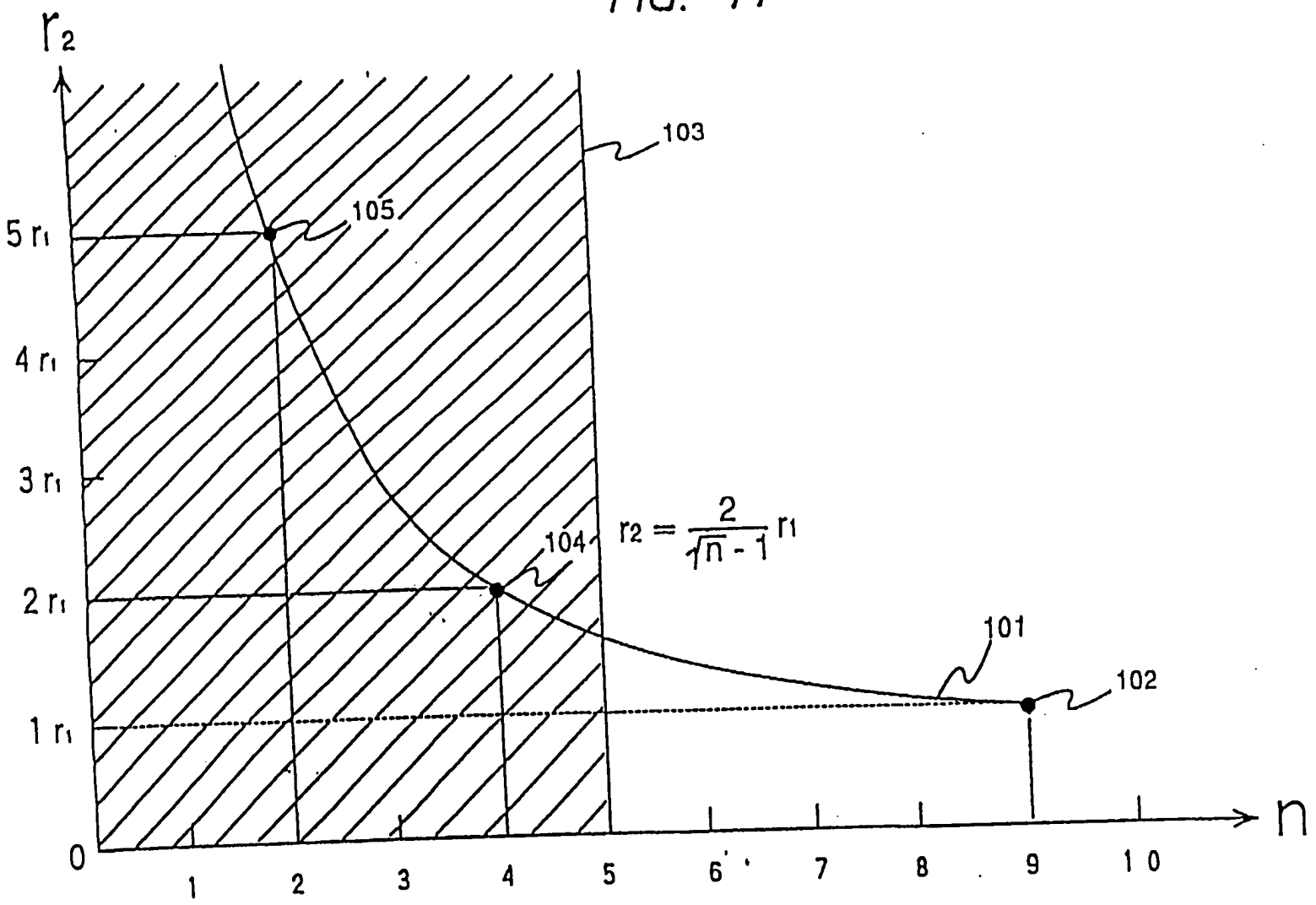

r2
5 r1
4 r1
3 r1
2 r1
1 r1
0
1
2
3
4
5
6
7
8
9
10
n
103
105
104
101
102
r2 = 2/√n - 1 r1

FIG. 12

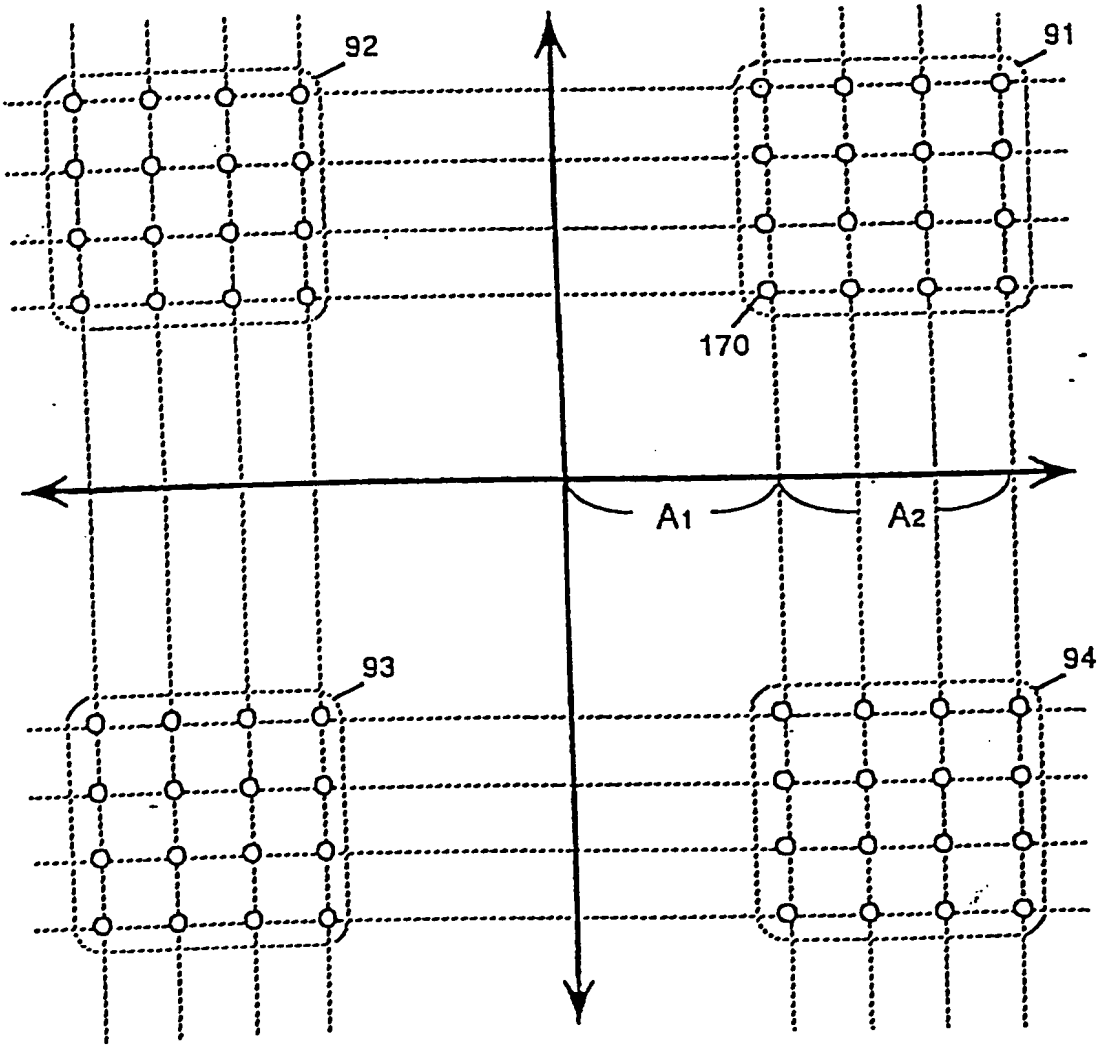


FIG. 13

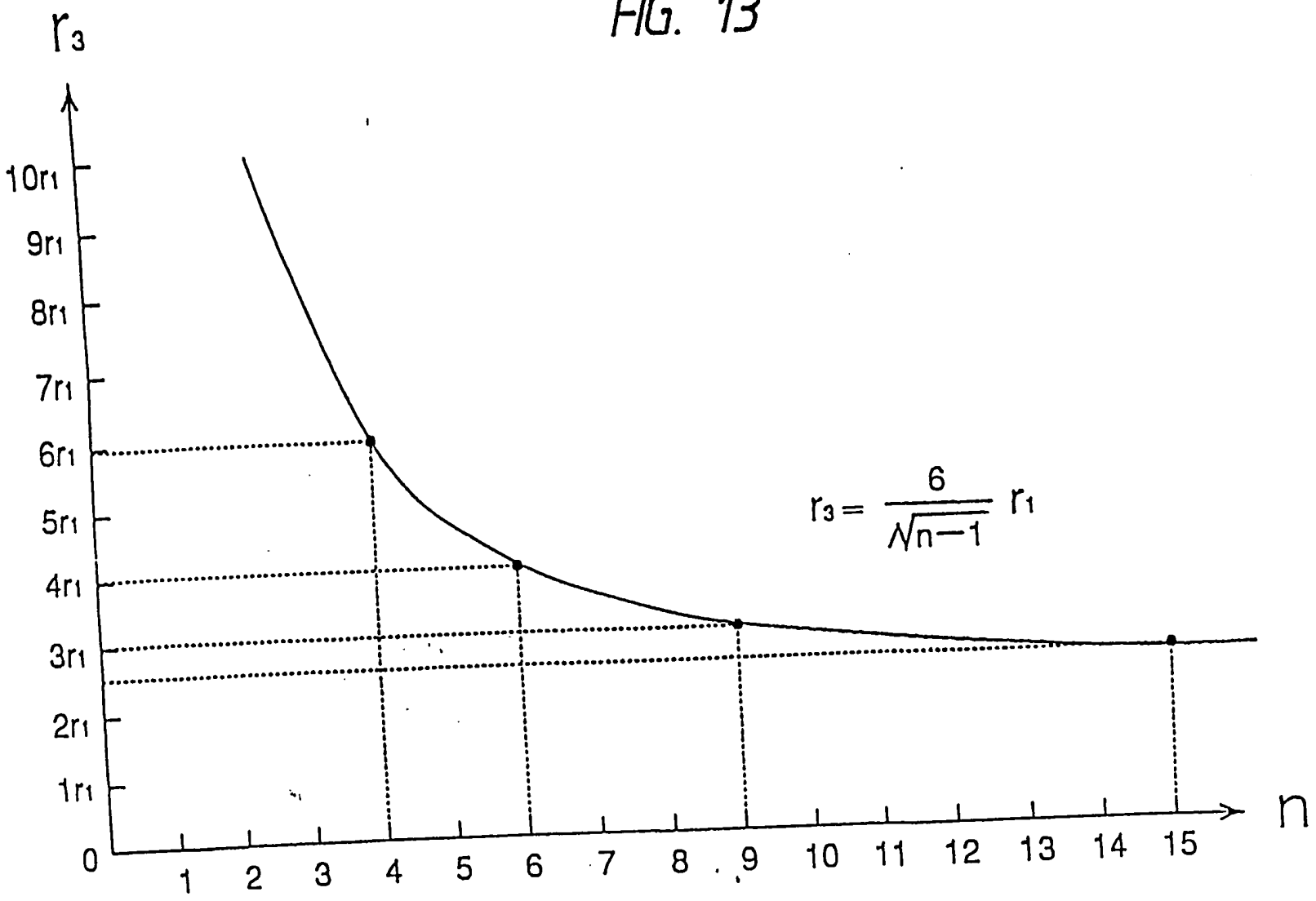

r_3
10r1
9r1
8r1
7r1
6r1
5r1
4r1
3r1
2r1
1r1
0
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
n
$r_3 = \frac{6}{\sqrt{n-1}} r_1$

FIG. 14

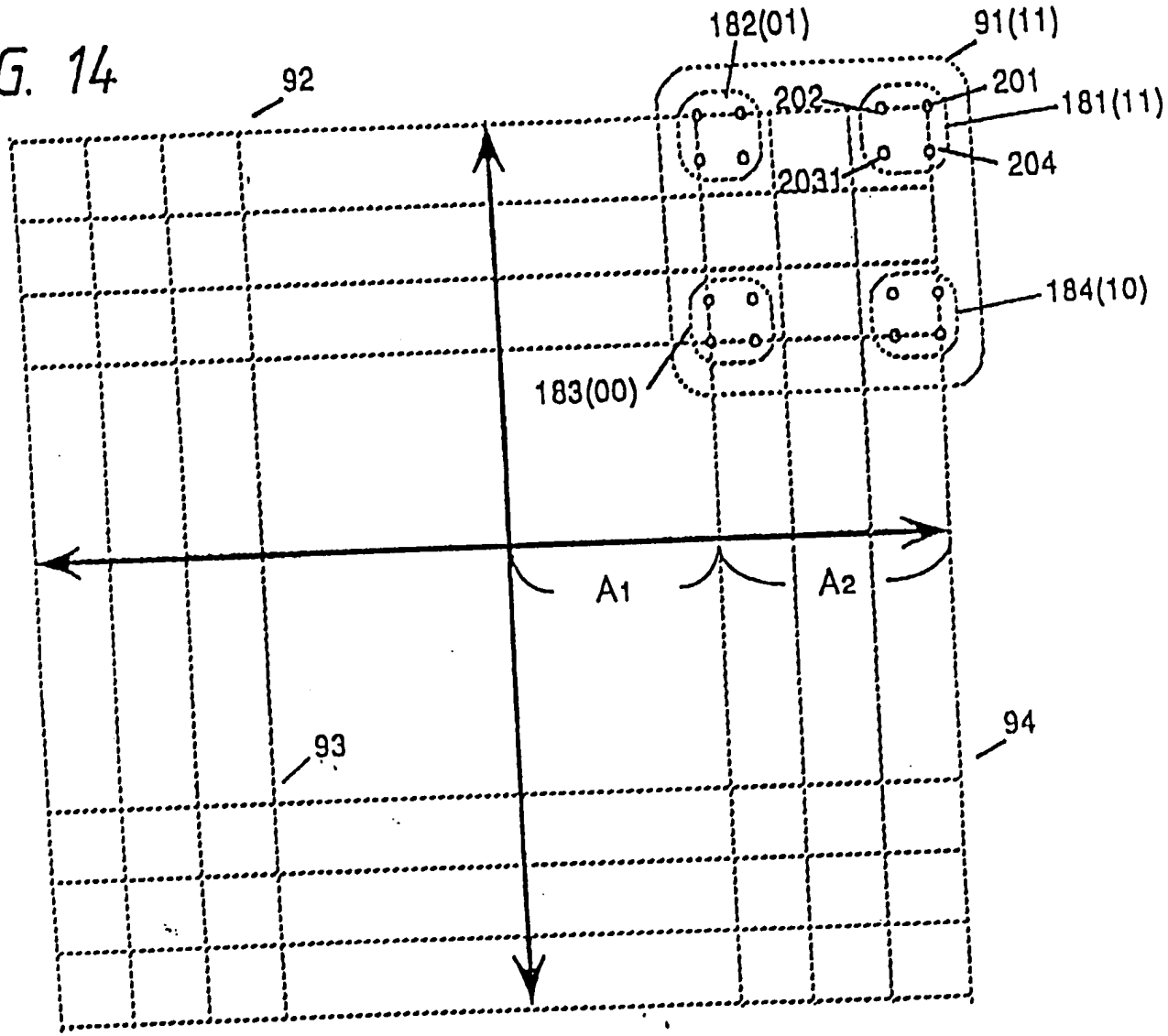


FIG. 15

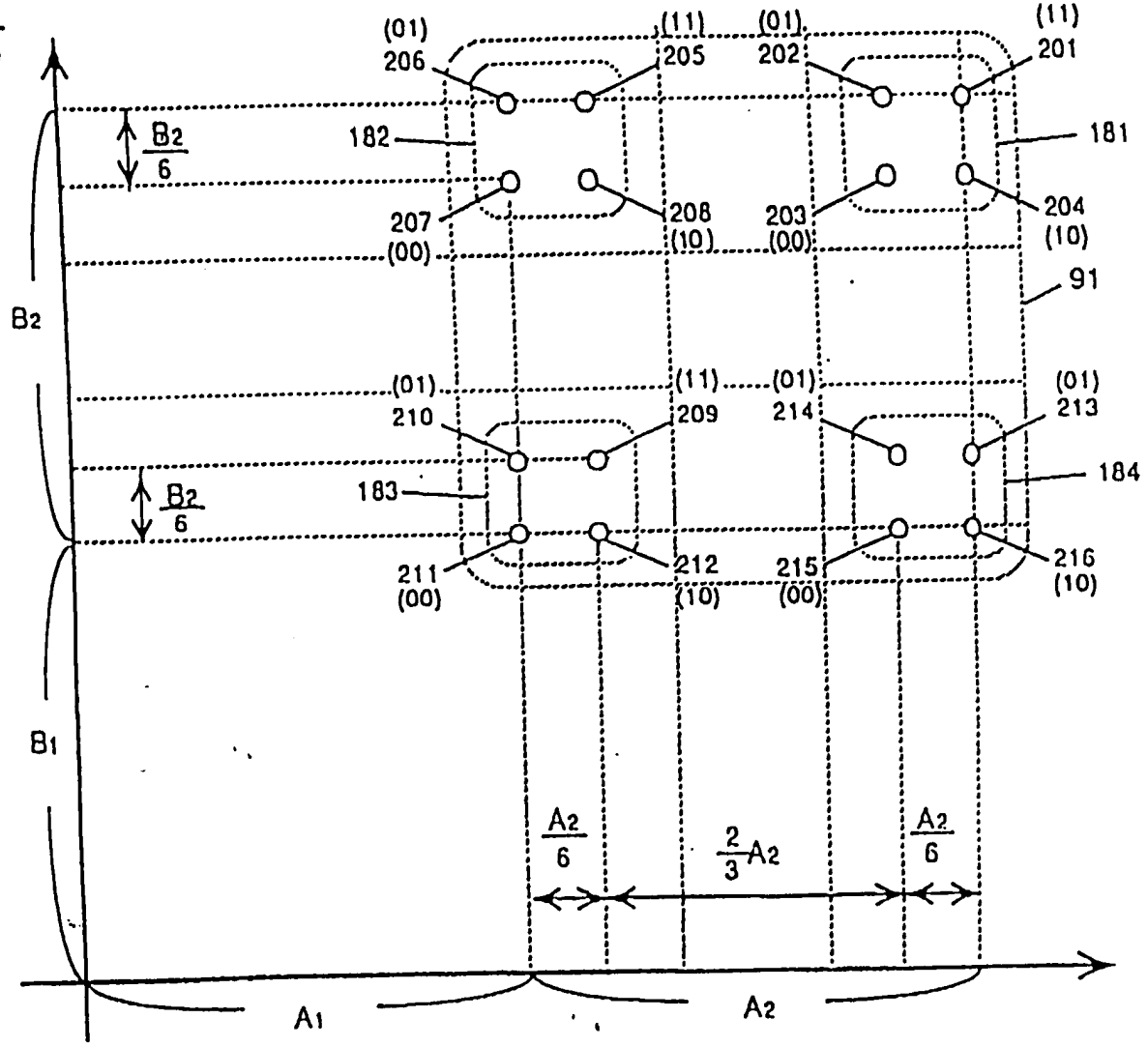

(01)
206
(11)
205
(01)
202
(11)
201
182
181
B2/6
207
208
(10)
203
(00)
204
(10)
(00)
91
B2
(01)
(11)
(01)
(01)
210
209
214
213
184
183
B2/6
211
(00)
212
(10)
215
(00)
216
(10)
B1
A2/6
2/3 A2
A2/6
A1
A2

FIG. 16

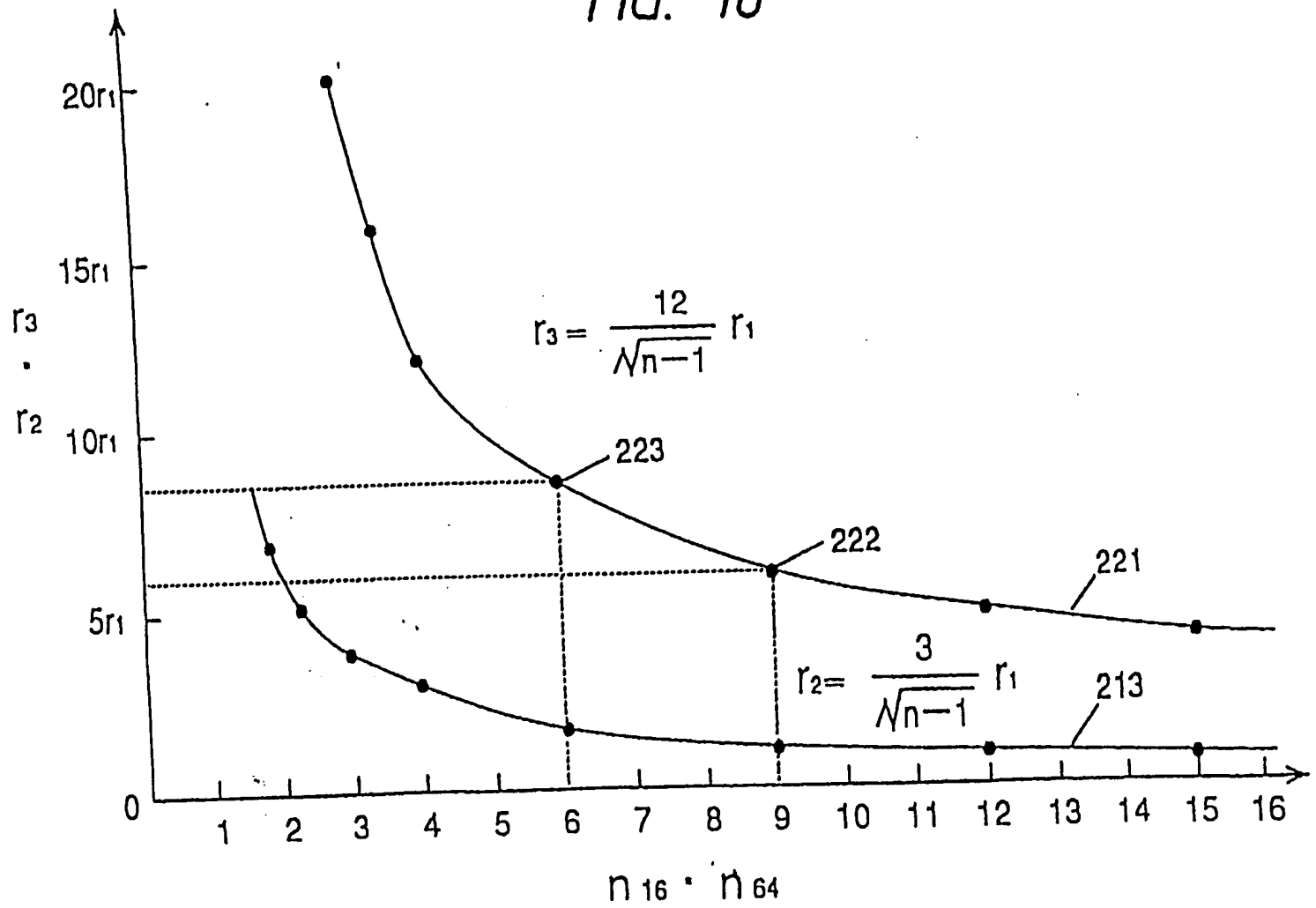

20r1
15r1
10r1
5r1
0
r3
r2
r3 = 12 / √(n−1) r1
r2 = 3 / √(n−1) r1
223
222
221
213
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
n16 · n64

FIG. 17

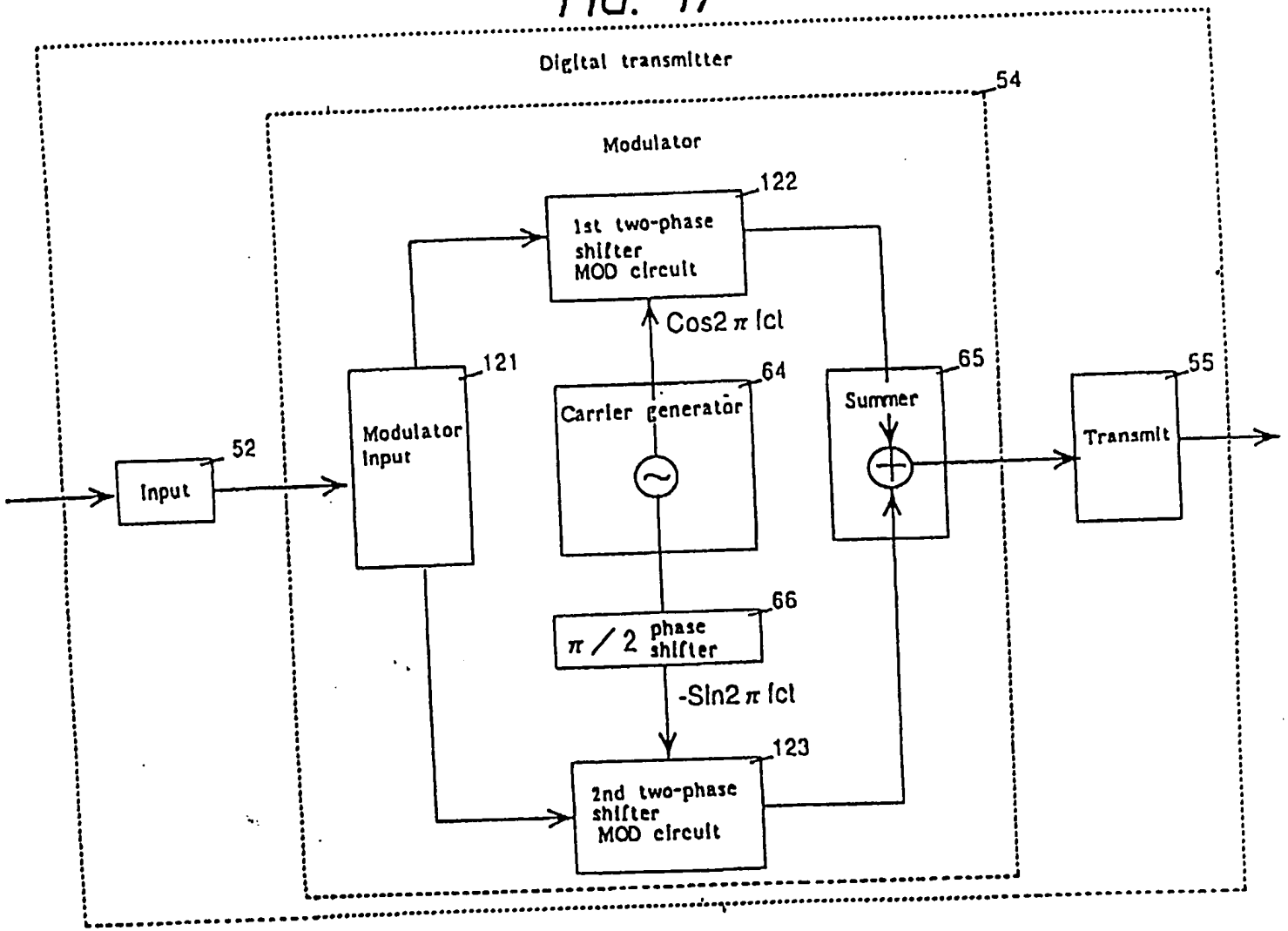

Digital transmitter
54
Modulator
122
1st two-phase shifter MOD circuit
Cos2πfct
121
64
65
55
Modulator Input
Carrier generator
Summer
Transmit
52
Input
66
π/2 phase shifter
-Sin2πfct
123
2nd two-phase shifter MOD circuit

FIG. 18

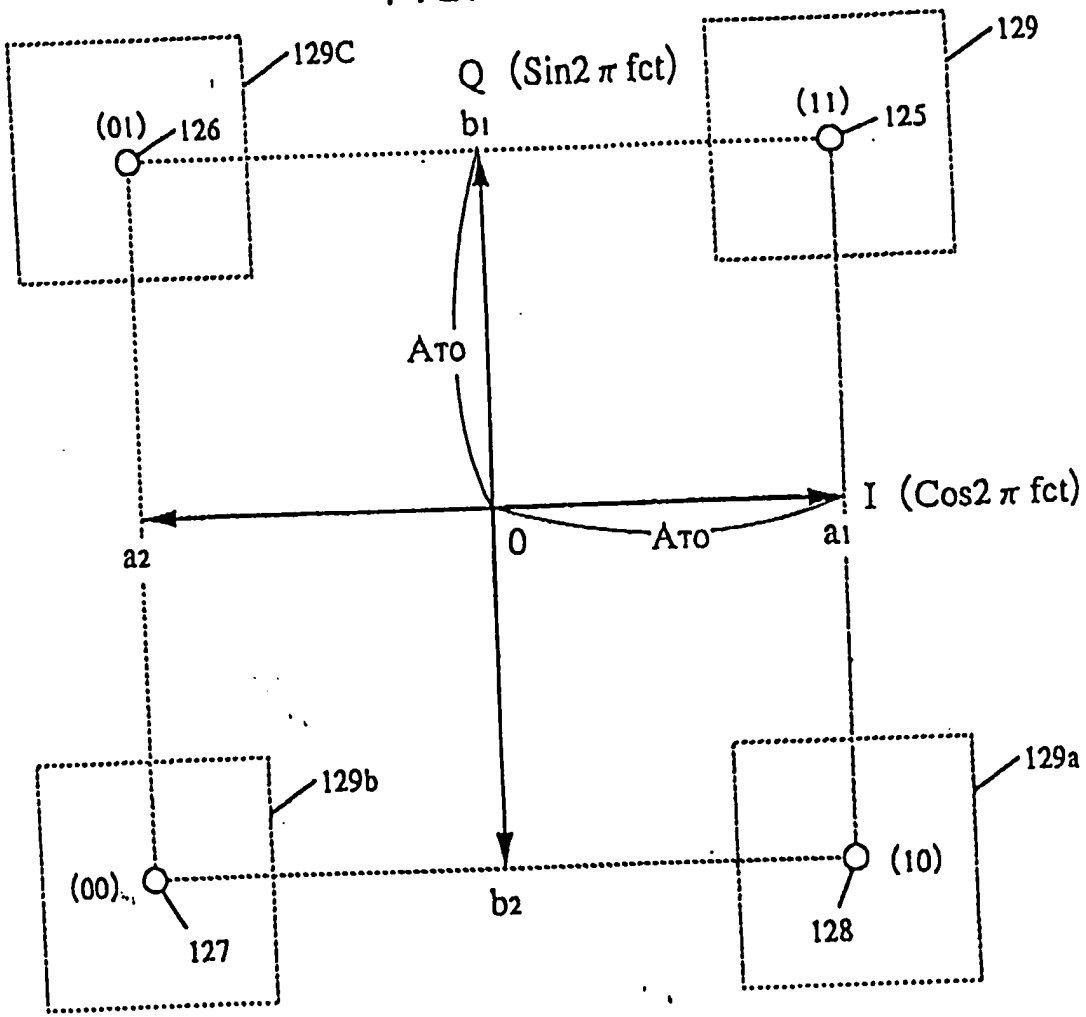

129C
Q (Sin2 π fct)
129
(01)
126
b1
(11)
125
ATO
I (Cos2 π fct)
a2
0
ATO
a1
129b
129a
(00)
127
b2
(10)
128

FIG. 19

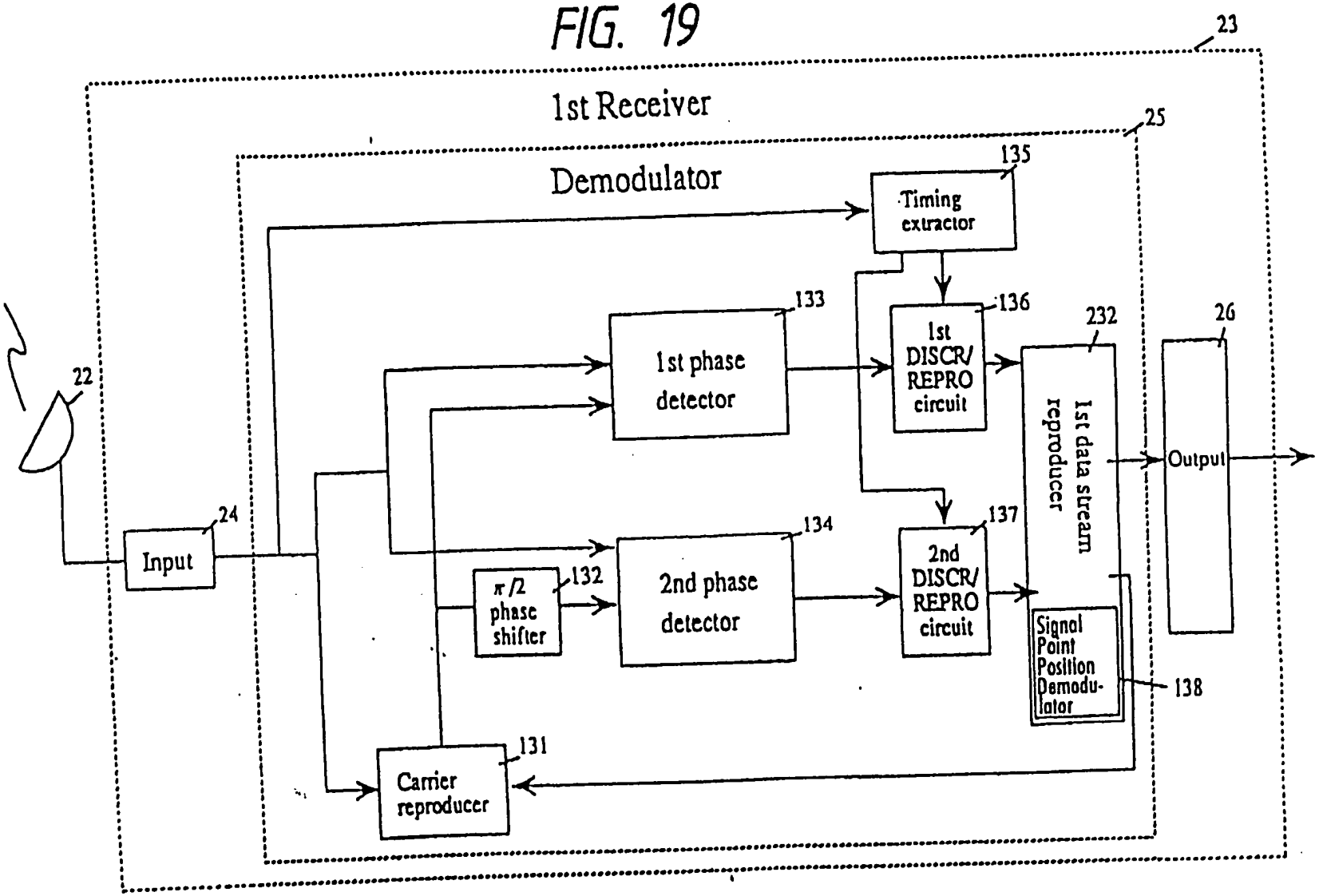

23
1st Receiver
25
Demodulator
135
Timing extractor
133
1st phase detector
136
1st DISCR/ REPRO circuit
232
1st data stream reproducer
26
Output
22
24
Input
134
2nd phase detector
137
2nd DISCR/ REPRO circuit
π/2 phase shifter
132
Signal Point Position Demodu-lator
138
131
Carrier reproducer

FIG. 20

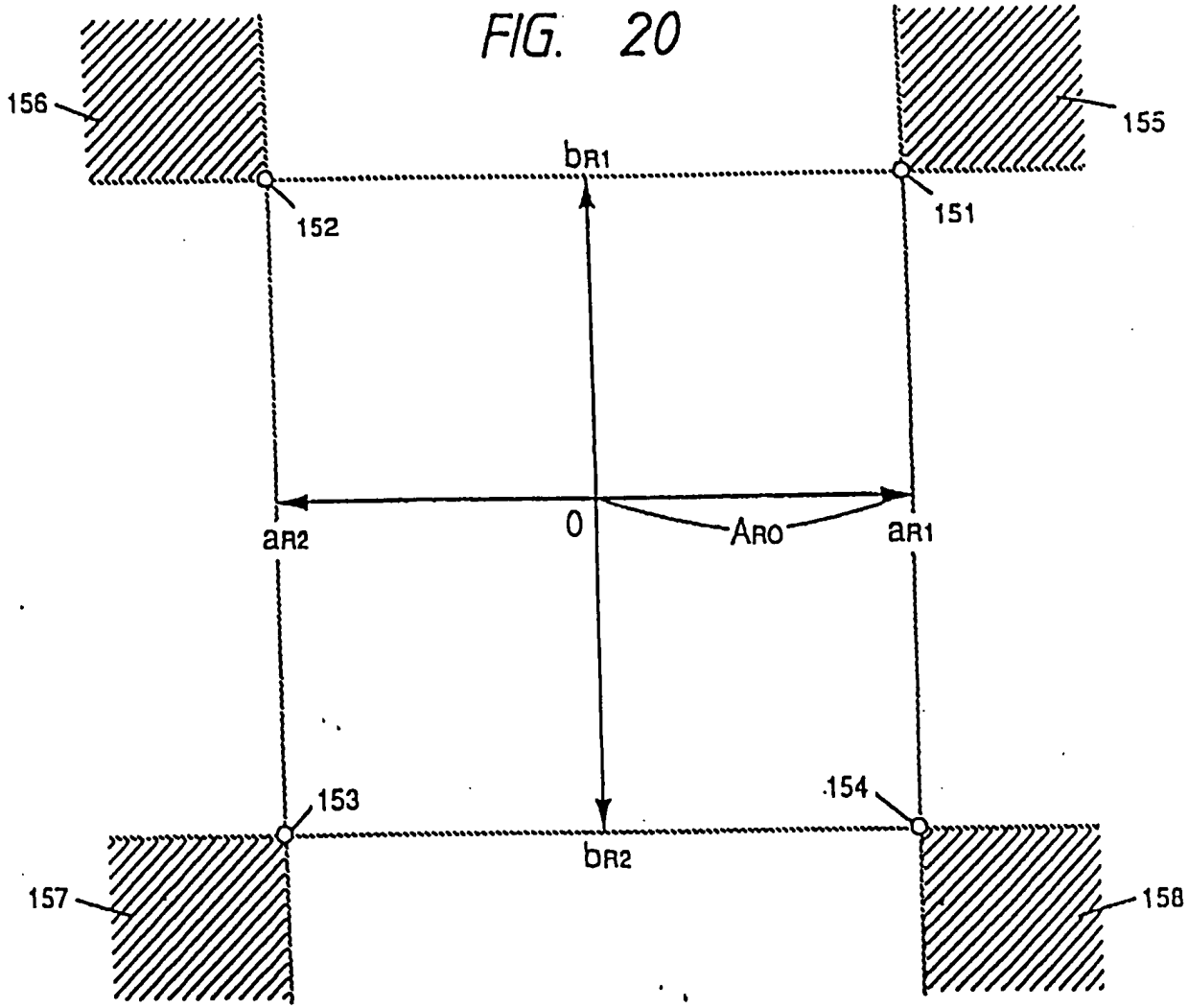


FIG. 21

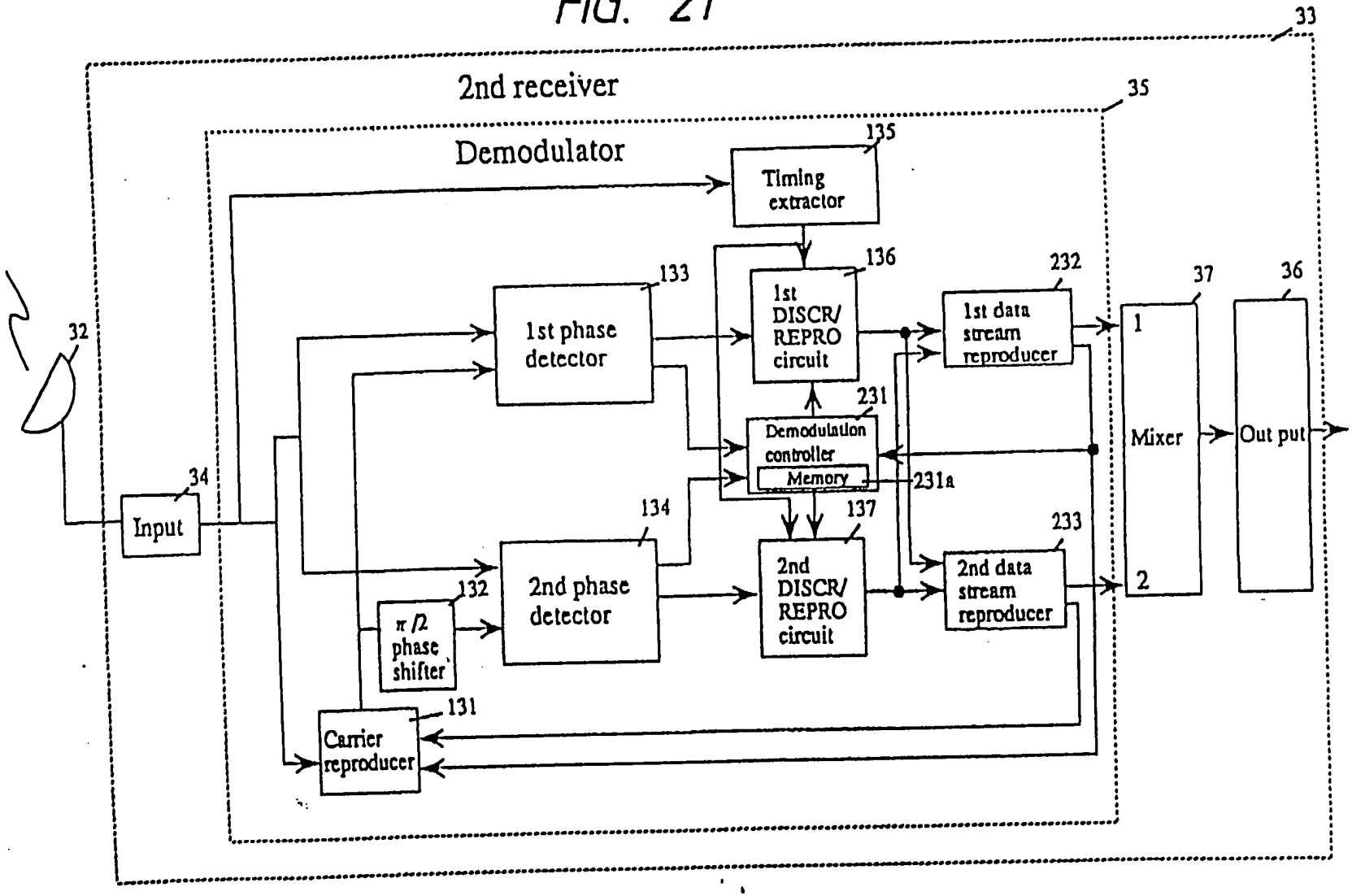

33
2nd receiver
35
Demodulator
135
Timing extractor
136
1st DISCR/ REPRO circuit
133
1st phase detector
232
1st data stream reproducer
37
36
32
231
Demodulation controller
Memory
231a
Mixer
Out put
1
2
34
Input
134
137
233
2nd phase detector
2nd DISCR/ REPRO circuit
2nd data stream reproducer
132
π/2 phase shifter
131
Carrier reproducer

FIG. 22

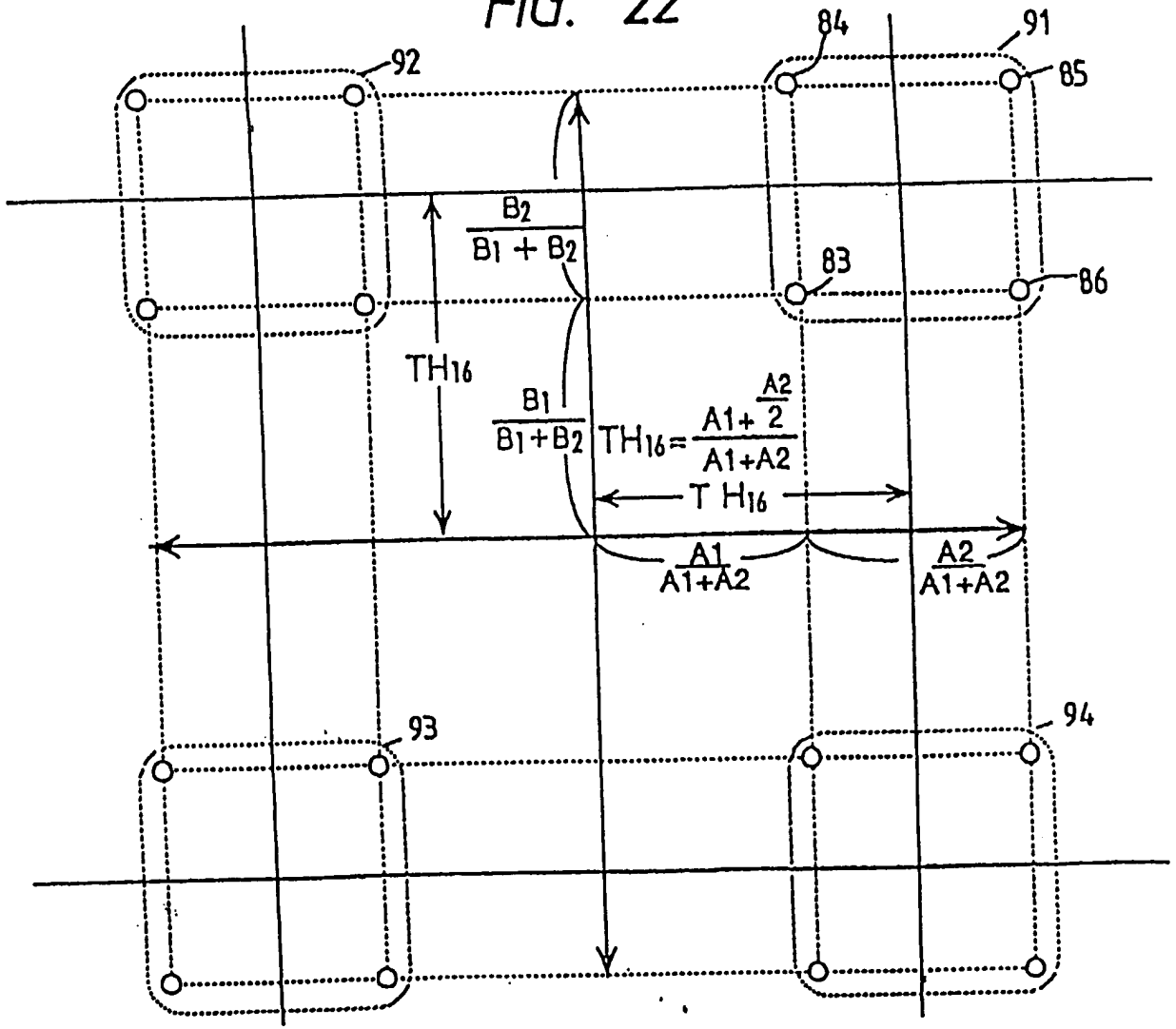

92
84
91
85
$\frac{B_2}{B_1 + B_2}$
83
86
TH_{16}
$\frac{B_1}{B_1+B_2}$ $TH_{16} = \frac{A1 + \frac{A2}{2}}{A1+A2}$
$T H_{16}$
$\frac{A1}{A1+A2}$
$\frac{A2}{A1+A2}$
93
94

FIG. 23

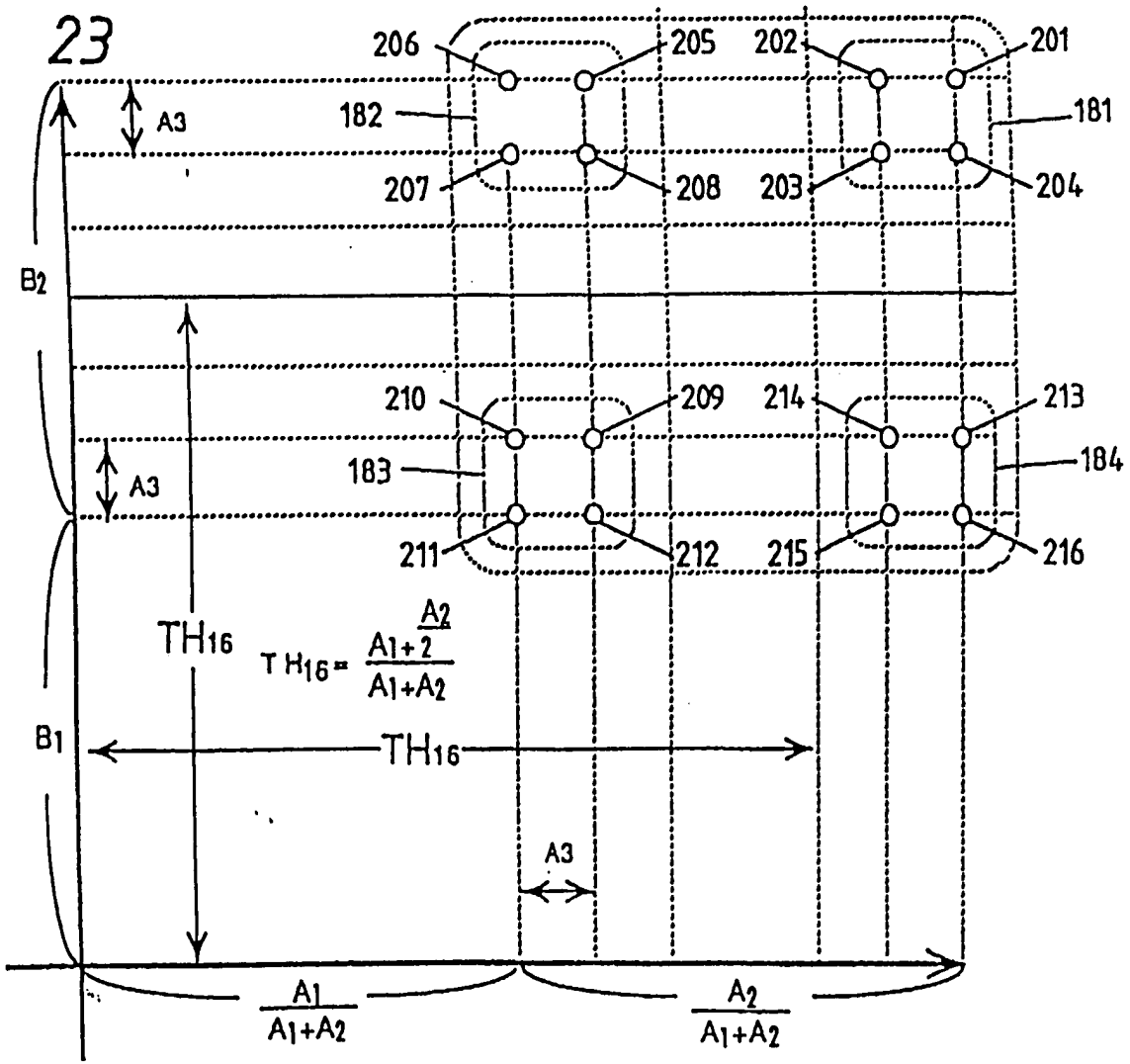

206
205
202
201
182
181
A3
207
208
203
204
B2
210
209
214
213
183
184
A3
211
212
215
216
TH16
TH16 = A2 / A1+2 / A1+A2
B1
TH16
A3
A1 / A1+A2
A2 / A1+A2

FIG. 24

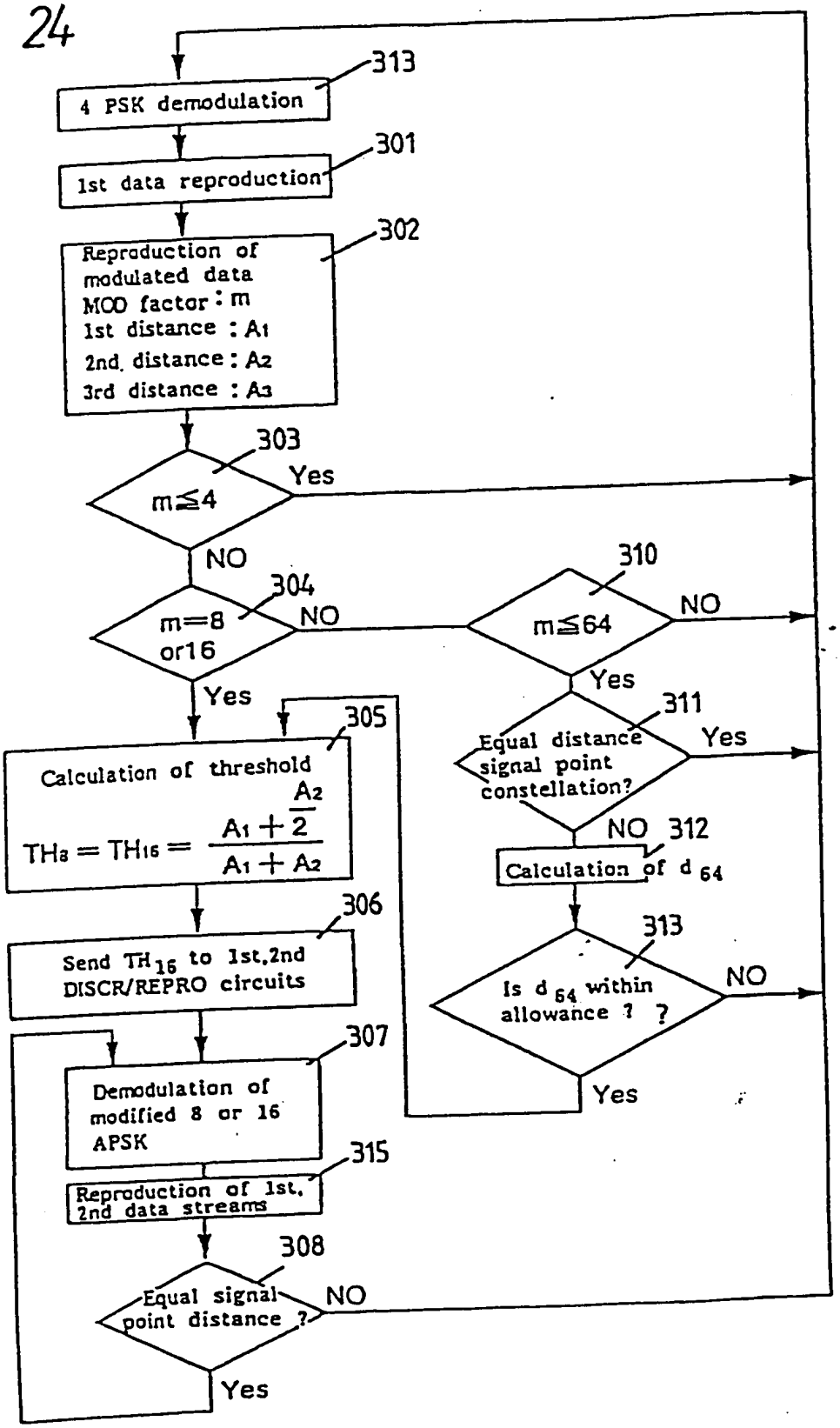

313
4 PSK demodulation
301
1st data reproduction
302
Reproduction of modulated data
MOD factor : m
1st distance : A1
2nd. distance : A2
3rd distance : A3
303
m≦4
Yes
NO
304
m=8 or16
NO
Yes
310
m≦64
NO
Yes
311
Equal distance signal point constellation?
Yes
NO
312
Calculation of d64
313
Is d64 within allowance ? ?
NO
Yes
305
Calculation of threshold
TH8 = TH16 = (A1 + A2/2) / (A1 + A2)
306
Send TH16 to 1st,2nd DISCR/REPRO circuits
307
Demodulation of modified 8 or 16 APSK
315
Reproduction of 1st, 2nd data streams
308
Equal signal point distance ?
NO
Yes

FIG. 25(a)

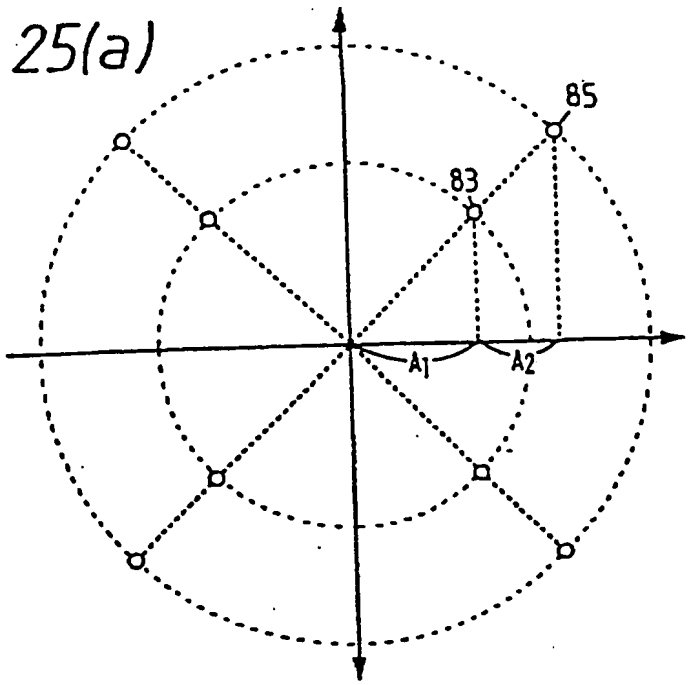


FIG. 25(b)

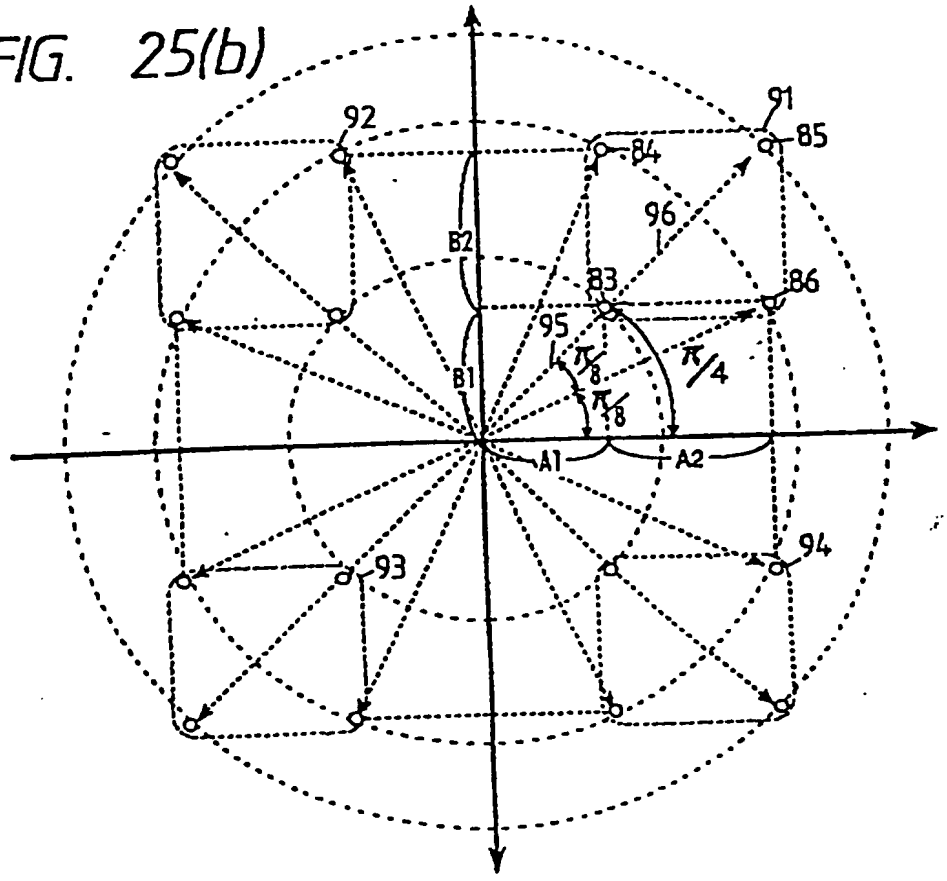


FIG. 26

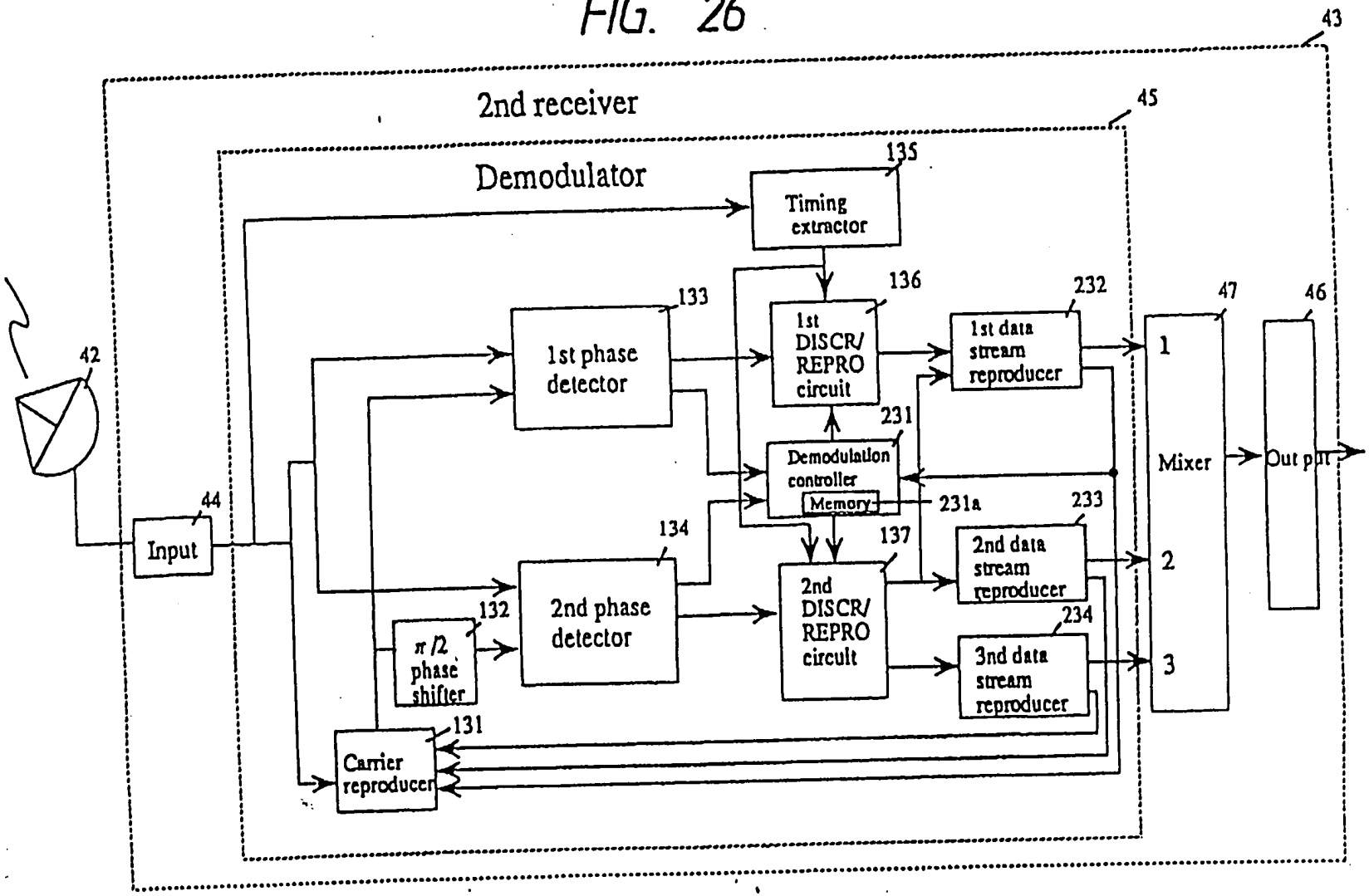

43
2nd receiver
45
Demodulator
135
Timing extractor
136
1st DISCR/ REPRO circuit
133
1st phase detector
232
1st data stream reproducer
47
46
42
231
Demodulation controller
Memory
231a
Mixer
Out put
44
Input
134
137
233
2nd data stream reproducer
2nd phase detector
2nd DISCR/ REPRO circuit
132
π/2 phase shifter
234
3nd data stream reproducer
131
Carrier reproducer
1
2
3

FIG. 27

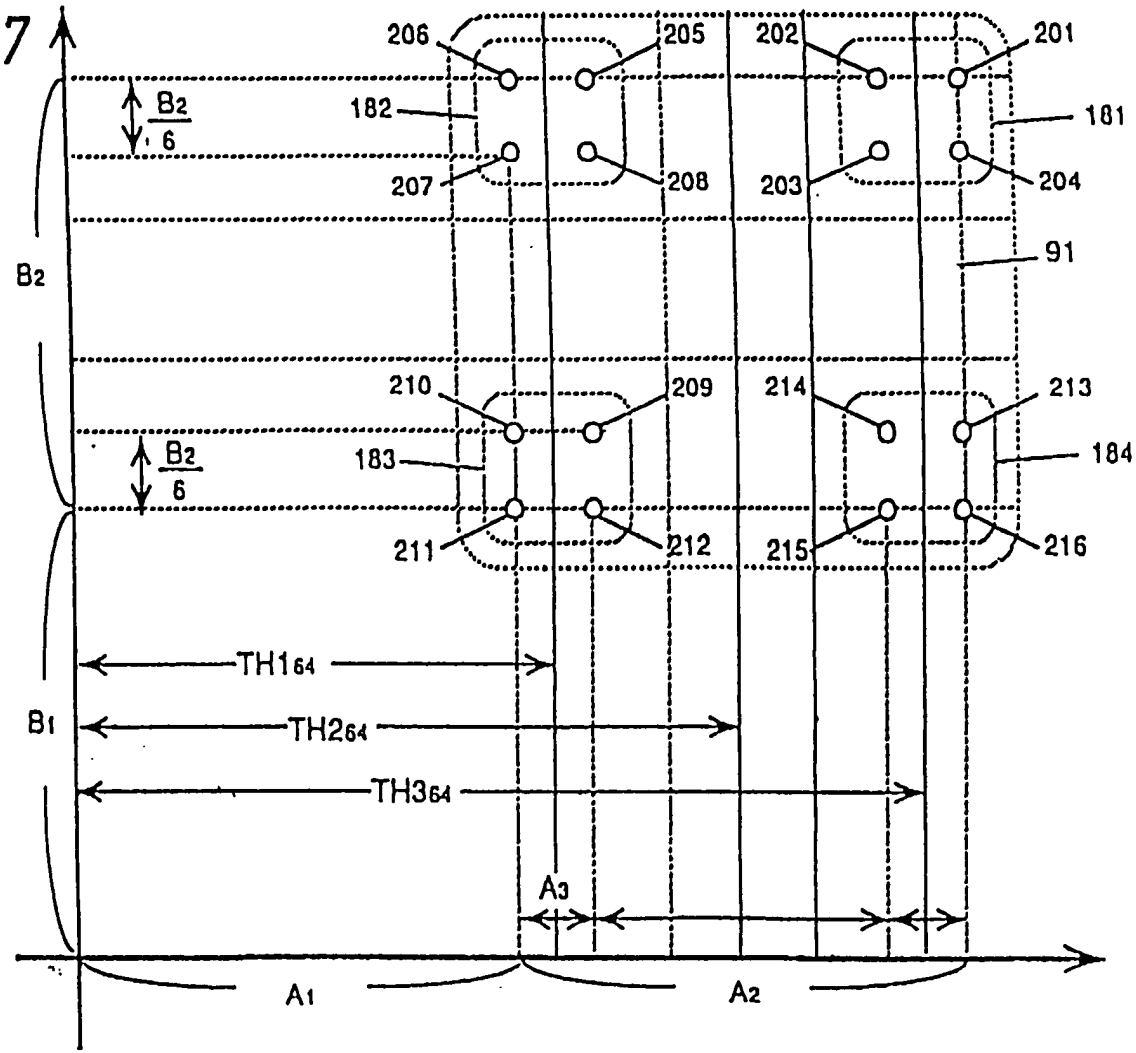

206
205
202
201
182
181
207
208
203
204
91
210
209
214
213
183
184
211
212
215
216
B2
B2/6
B2
B2/6
B1
TH164
TH264
TH364
A3
A1
A2

FIG. 28

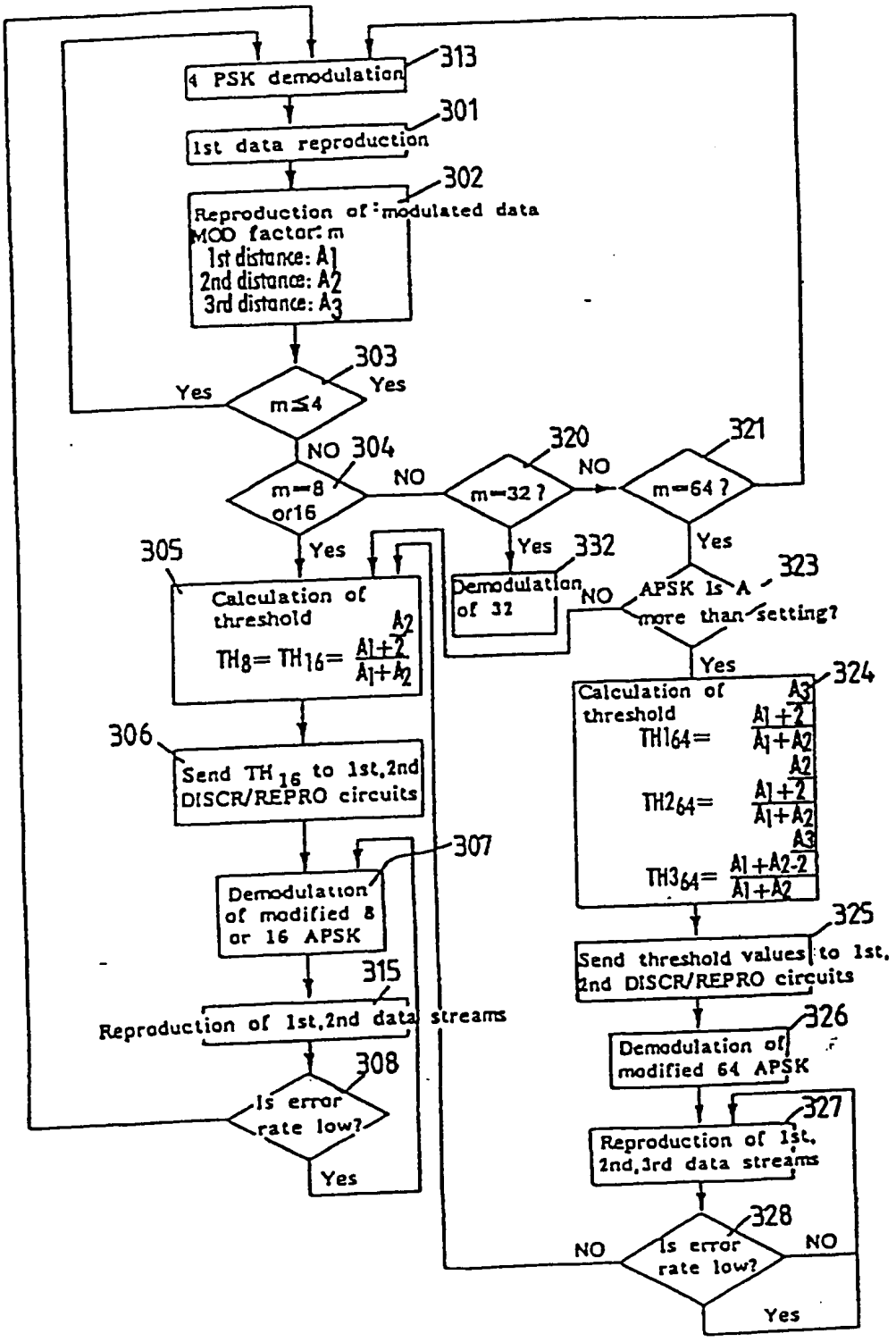

4 PSK demodulation
313
1st data reproduction
301
Reproduction of modulated data
MOD factor: m
1st distance: A1
2nd distance: A2
3rd distance: A3
302
m≤4
303
Yes
NO
m=8 or16
304
NO
m=32 ?
320
NO
m=64 ?
321
Yes
Yes
Yes
305
Calculation of threshold
TH8= TH16= A2 / A1+A2
Demodulation of 32
332
APSK Is A more than setting?
323
NO
Yes
306
Send TH16 to 1st,2nd DISCR/REPRO circuits
Calculation of threshold
TH164= A3 / A1+A2
TH264= A2 / A1+A2
TH364= A3 / A1+A2-2
324
307
Demodulation of modified 8 or 16 APSK
Send threshold values to 1st, 2nd DISCR/REPRO circuits
325
315
Reproduction of 1st,2nd data streams
Demodulation of modified 64 APSK
326
308
Is error rate low?
Reproduction of 1st, 2nd,3rd data streams
327
328
Is error rate low?
NO
NO
Yes
Yes

FIG. 29

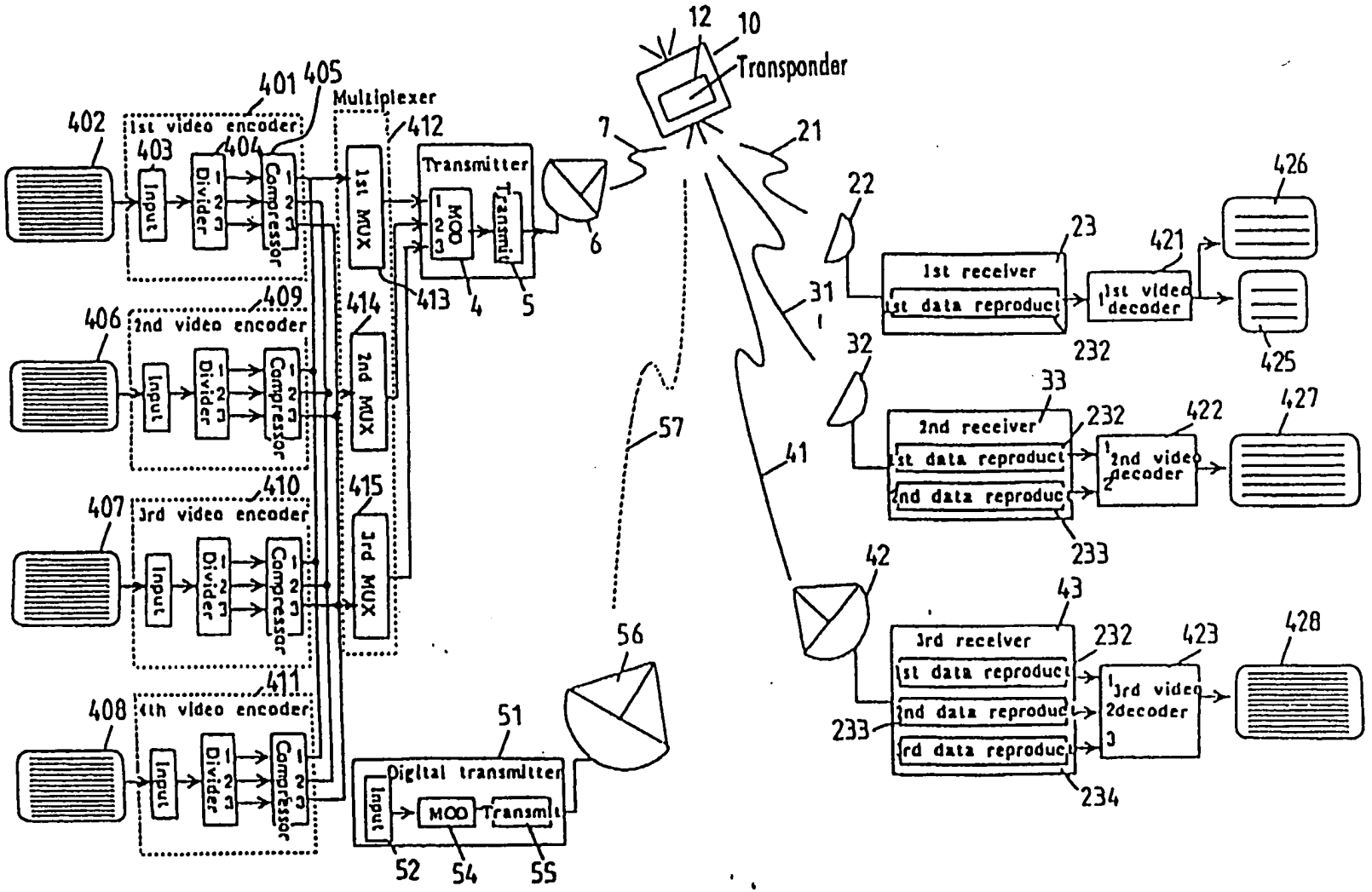

12
10
Transponder
401
405
Multiplexer
402
1st video encoder
403
404
412
Transmitter
7
21
426
22
1st receiver
23
421
1st video decoder
31
1st data reproduct
232
425
406
2nd video encoder
409
414
2nd MUX
32
33
2nd receiver
232
422
427
1st data reproduct
2nd data reproduc
233
407
3rd video encoder
410
415
3rd MUX
42
43
3rd receiver
232
423
428
1st data reproduct
2nd data reproduc
3rd data reproduc
233
234
408
Xth video encoder
411
Input
Divider
Compressor
MOD
Transmit
413
4
5
6
41
57
56
51
Digital transmitter
52
54
55

FIG. 30

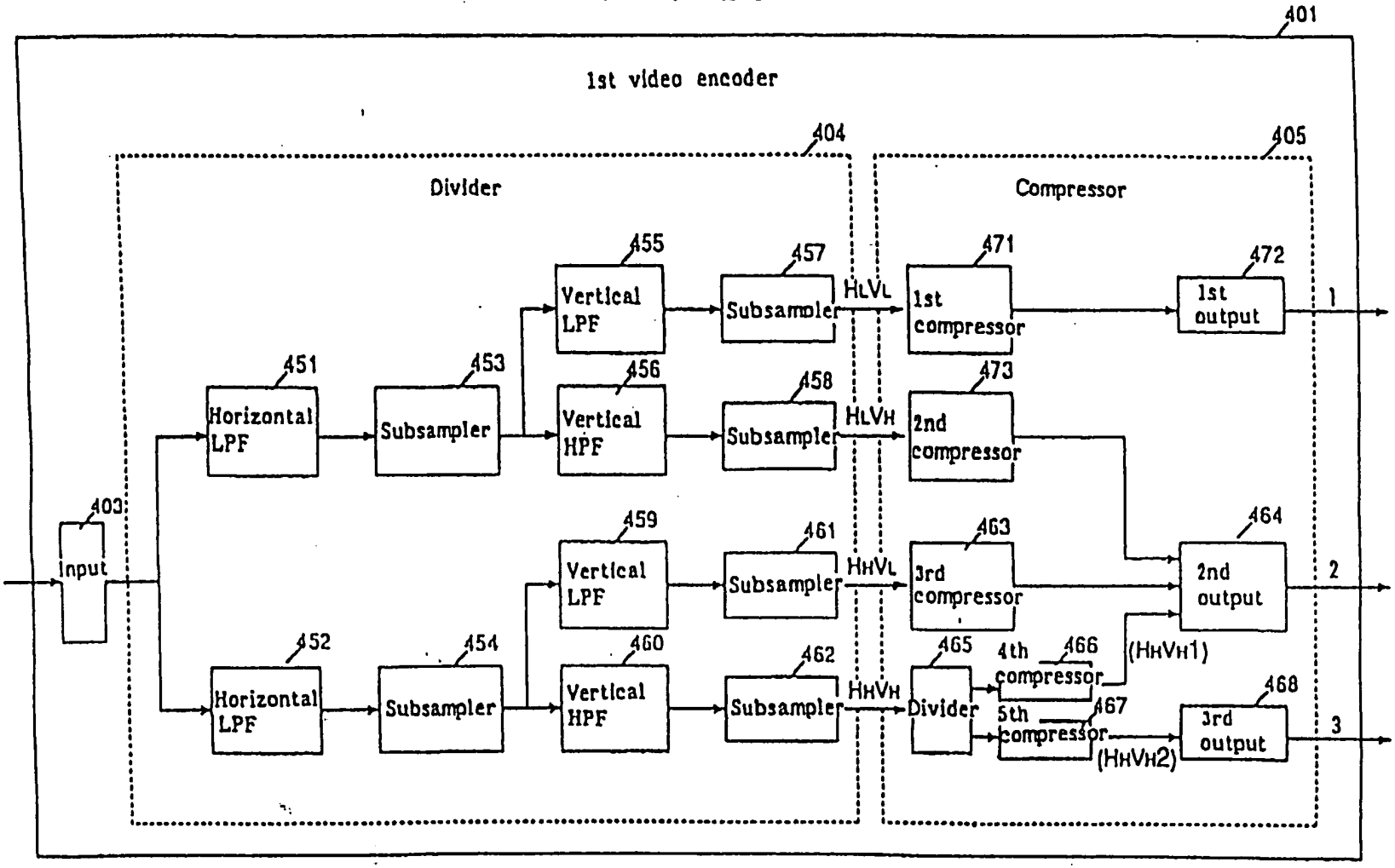

401
1st video encoder
404
Divider
405
Compressor
403
Input
451
Horizontal LPF
453
Subsampler
455
Vertical LPF
456
Vertical HPF
457
Subsampler
458
Subsampler
459
Vertical LPF
460
Vertical HPF
461
Subsampler
462
Subsampler
452
Horizontal LPF
454
Subsampler
HLVL
HLVH
HHVL
HHVH
471
1st compressor
473
2nd compressor
463
3rd compressor
465
Divider
466
4th compressor
467
5th compressor
472
1st output
464
2nd output
468
3rd output
1
2
3
(HHVH1)
(HHVH2)

FIG. 31

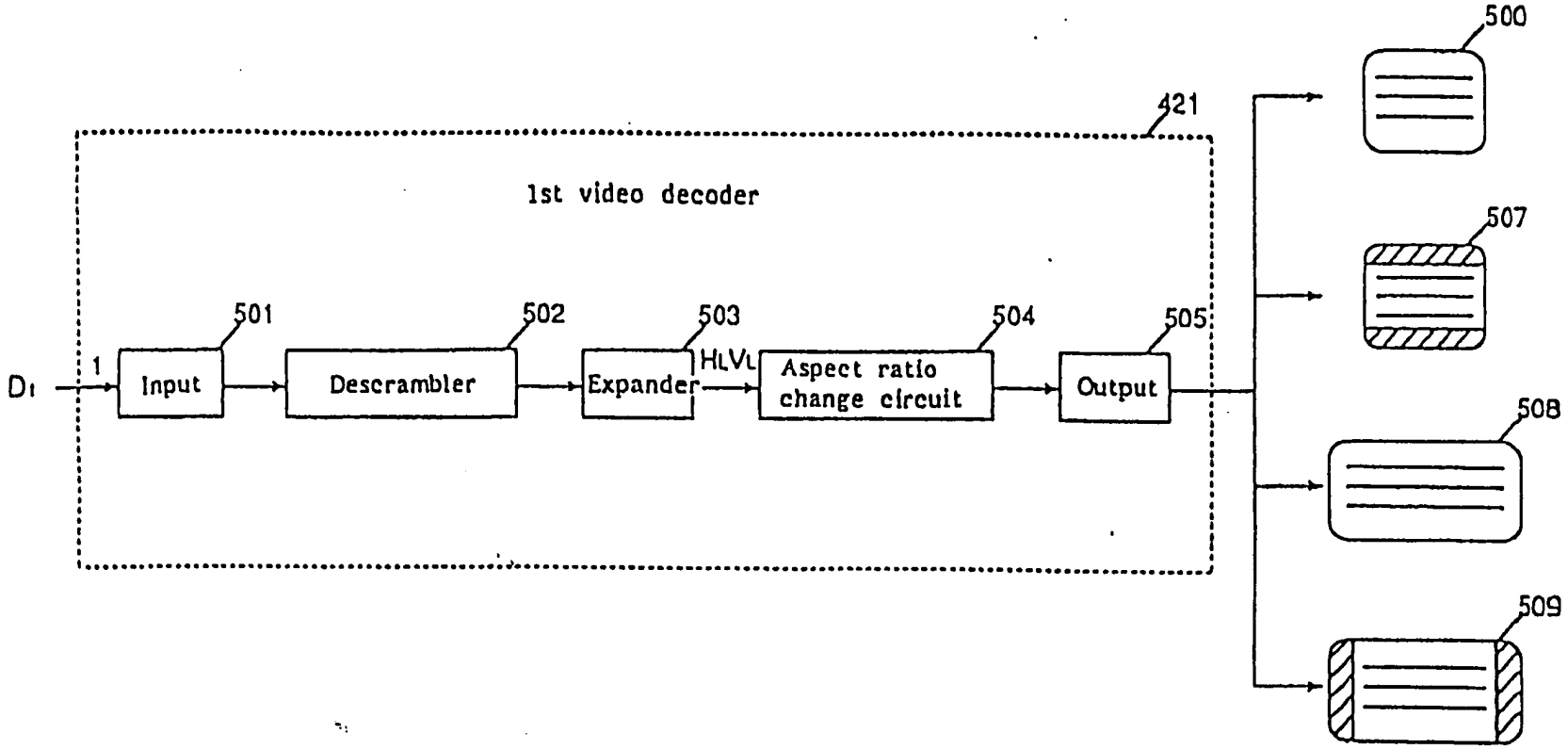

421
1st video decoder
501
502
503
504
505
1
Input
Descrambler
Expander
HLVL
Aspect ratio change circuit
Output
D1
500
507
508
509

FIG. 32

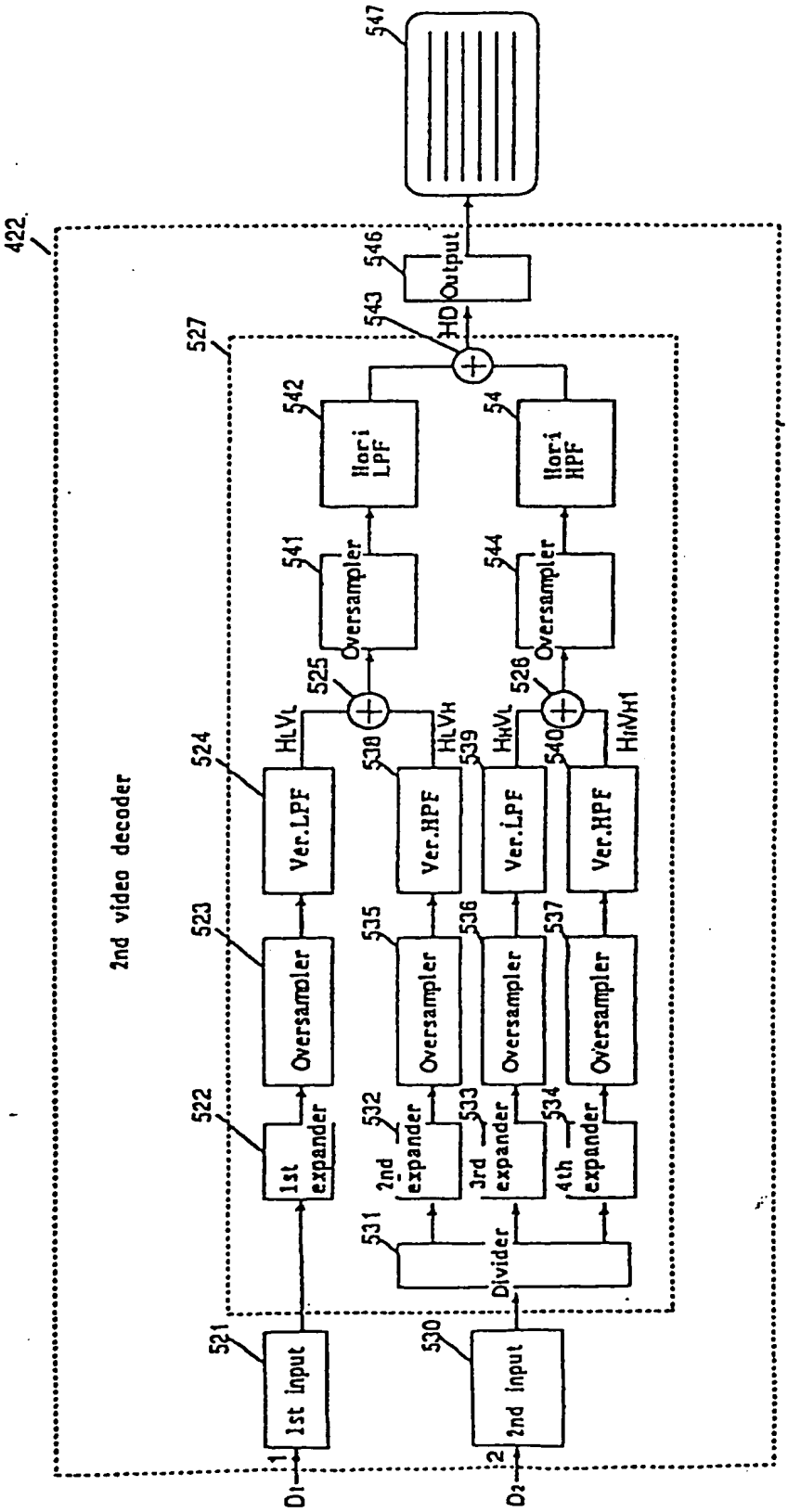

422
2nd video decoder
1
2
D1
D2
521
1st input
530
2nd input
522
1st expander
523
Oversampler
524
Ver.LPF
HLVL
525
Oversampler
541
Hori LPF
542
527
531
Divider
532
2nd expander
535
Oversampler
538
Ver.HPF
HLVH
533
3rd expander
536
Oversampler
539
Ver.LPF
HHVL
526
Oversampler
544
Hori HPF
54
534
4th expander
537
Oversampler
540
Ver.HPF
HHVH1
543
HD
546
Output
547

FIG. 33

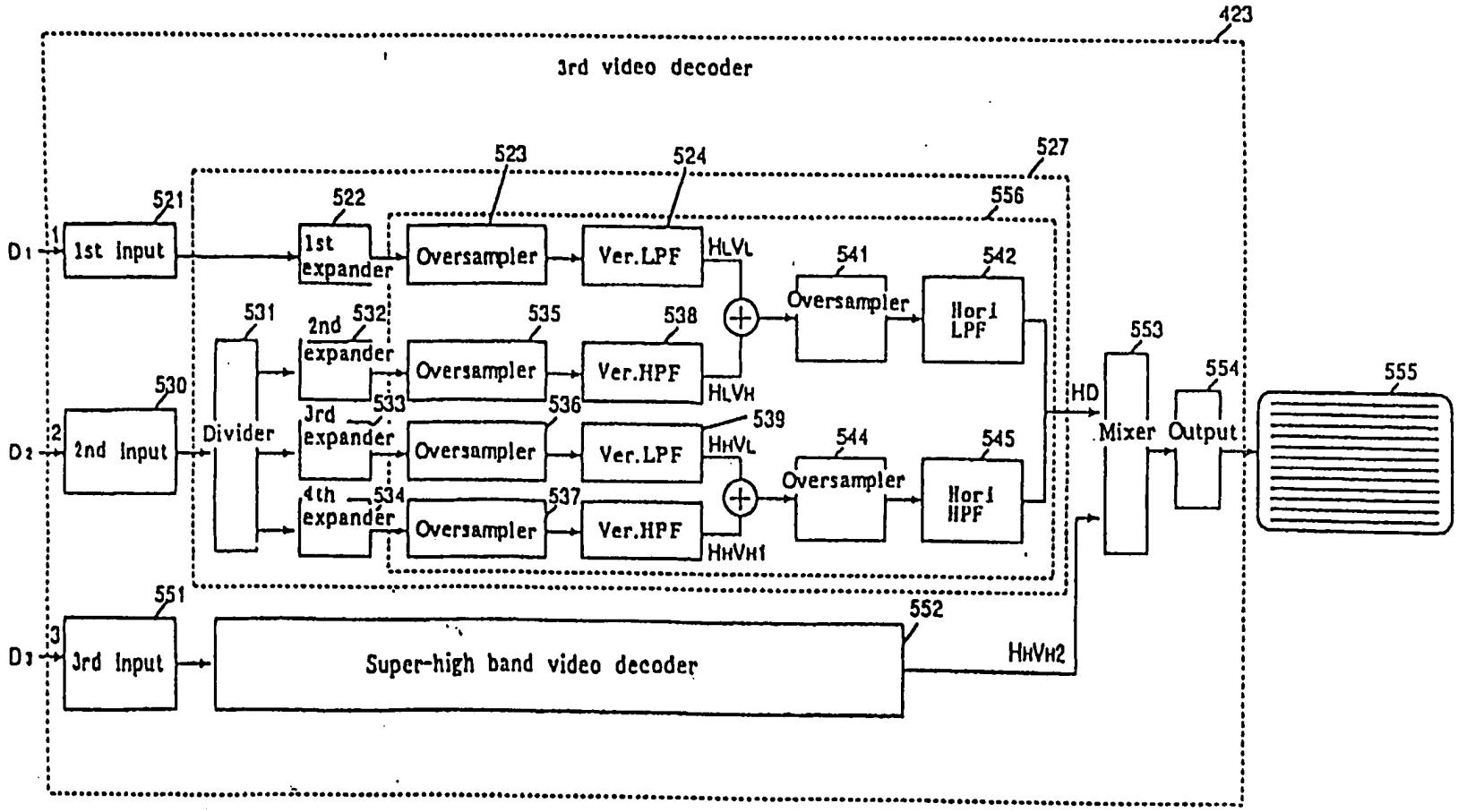

423
3rd video decoder
523
524
527
556
521
522
1st input
1st expander
Oversampler
Ver.LPF
HLVL
541
542
Oversampler
Hori LPF
531
2nd 532
expander
535
538
Oversampler
Ver.HPF
HLVH
530
553
554
555
HD
Mixer
Output
2nd input
Divider
3rd 533
expander
536
539
Oversampler
Ver.LPF
HHVL
544
545
4th 534
expander
537
Oversampler
Ver.HPF
HHVH1
Oversampler
Hori HPF
551
552
3rd Input
Super-high band video decoder
HHVH2
D1
D2
D3
1
2
3

FIG. 34

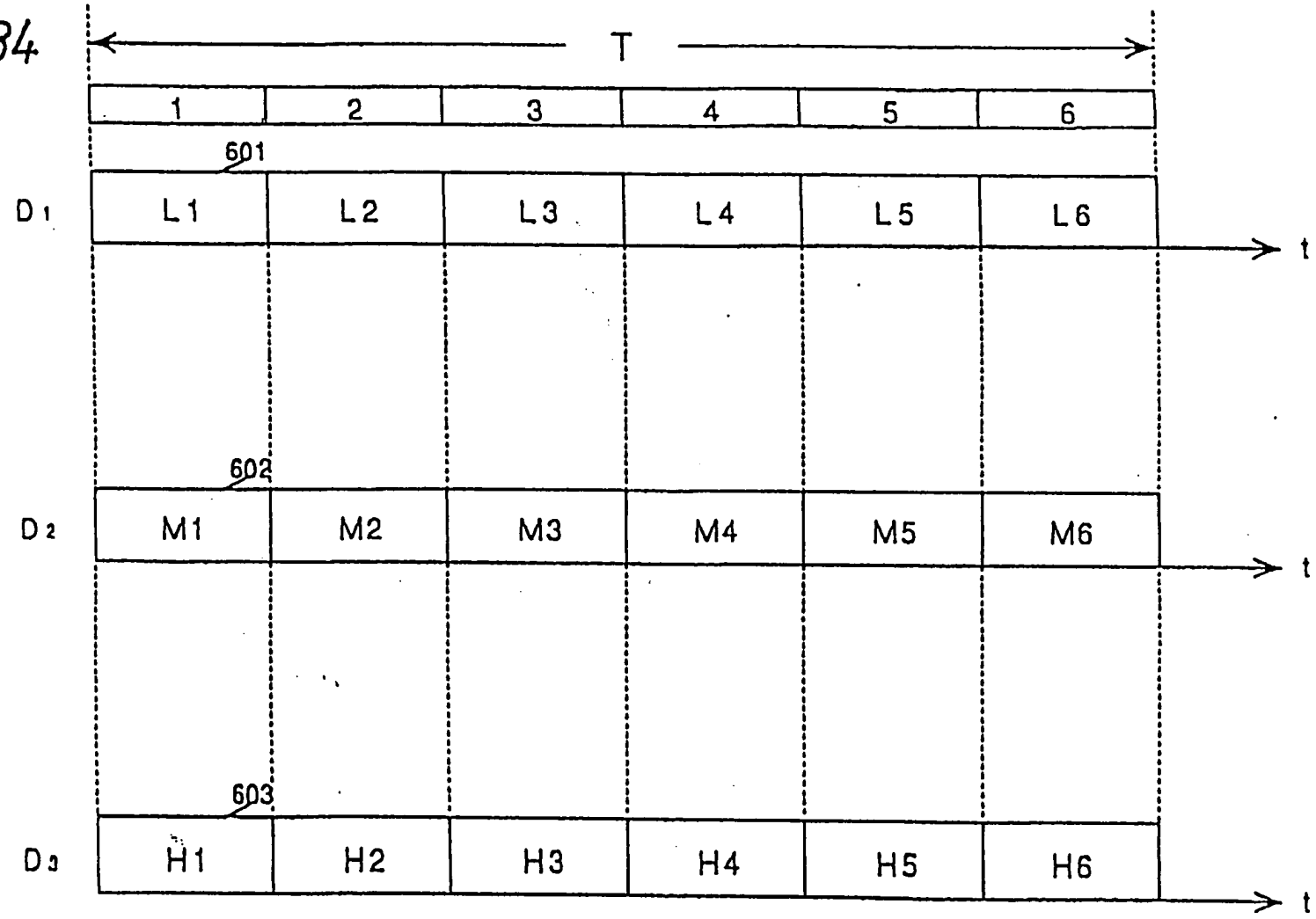

T
1
2
3
4
5
6
601
D1
L1
L2
L3
L4
L5
L6
t
602
D2
M1
M2
M3
M4
M5
M6
t
603
D3
H1
H2
H3
H4
H5
H6
t

FIG. 35

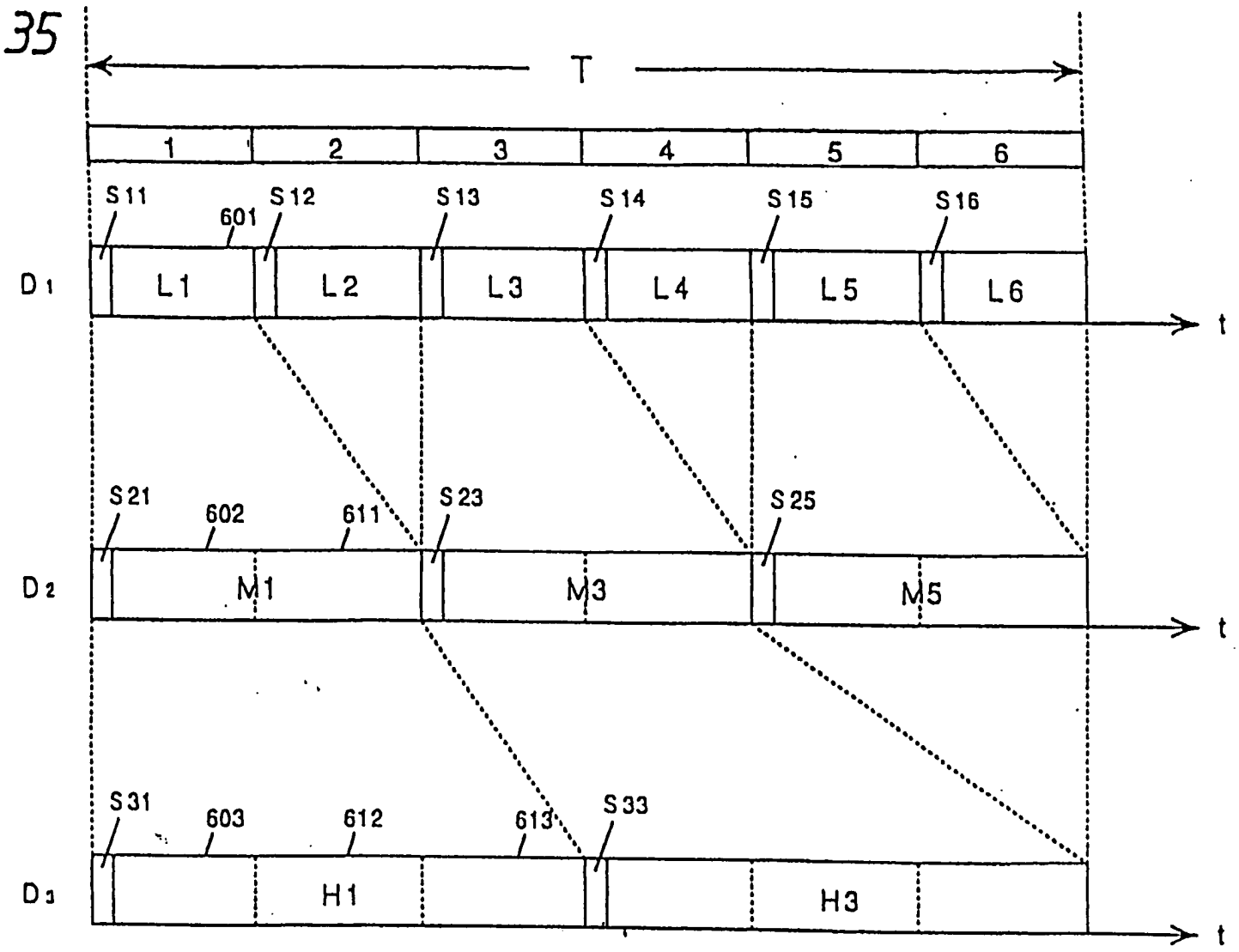

T
1
2
3
4
5
6
S11
601
S12
S13
S14
S15
S16
D1
L1
L2
L3
L4
L5
L6
t
S21
602
611
S23
S25
D2
M1
M3
M5
t
S31
603
612
613
S33
D3
H1
H3
t

FIG. 36

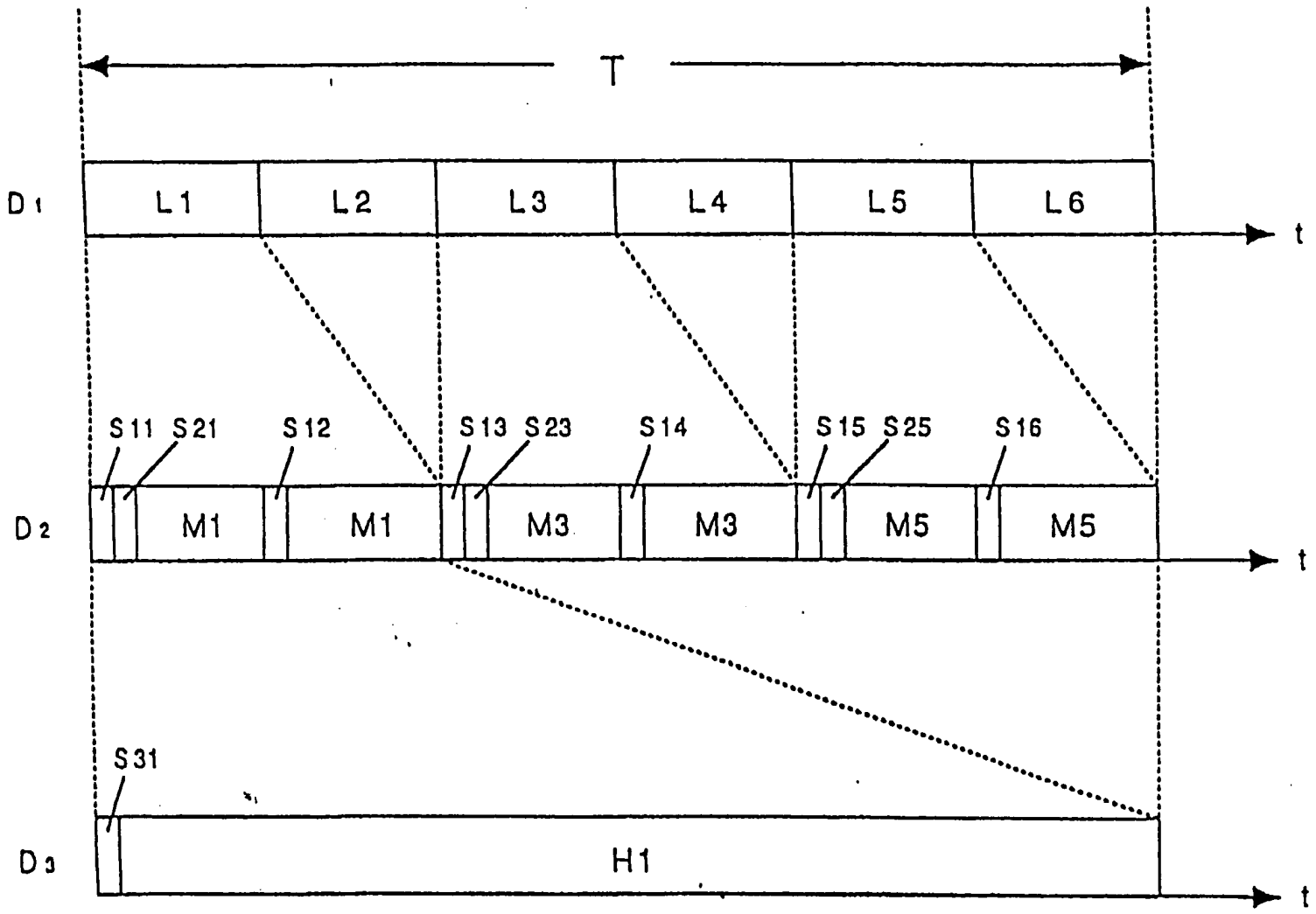

T
D1
L1
L2
L3
L4
L5
L6
t
S11
S21
S12
S13
S23
S14
S15
S25
S16
D2
M1
M1
M3
M3
M5
M5
t
S31
D3
H1
t

FIG. 37

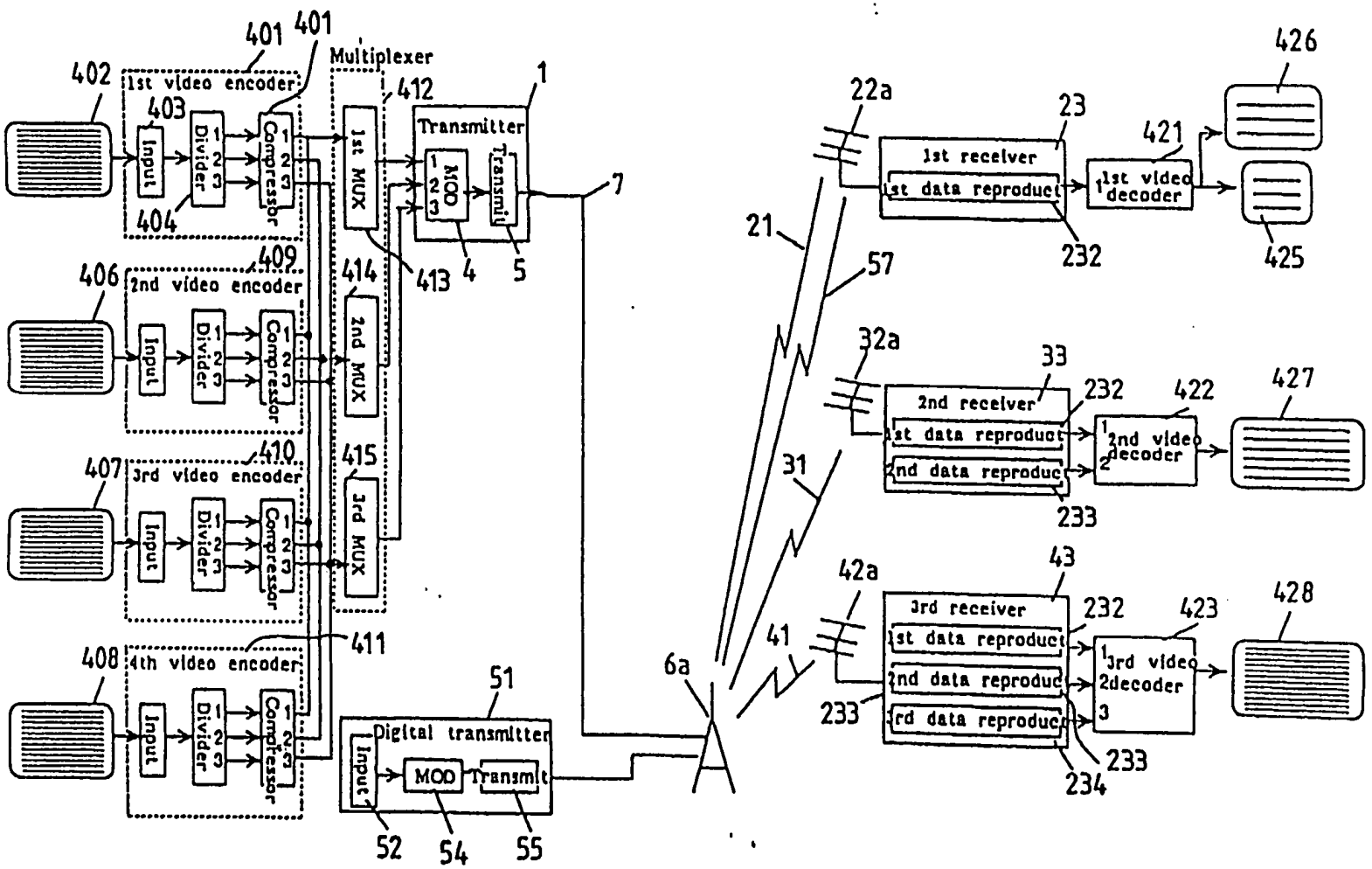

401
401
Multiplexer
402
1st video encoder
403
Input
Divider
Compressor
404
412
Transmitter
MOD
Transmit
1
7
1st MUX
413
4
5
406
409
2nd video encoder
414
2nd MUX
407
410
3rd video encoder
415
3rd MUX
408
411
4th video encoder
51
Digital transmitter
52
54
55
6a
21
57
31
41
22a
23
1st receiver
1st data reproduct
232
421
1st video decoder
426
425
32a
33
2nd receiver
2nd data reproduct
422
2nd video decoder
427
233
42a
43
3rd receiver
423
3rd video decoder
428
234

FIG. 38

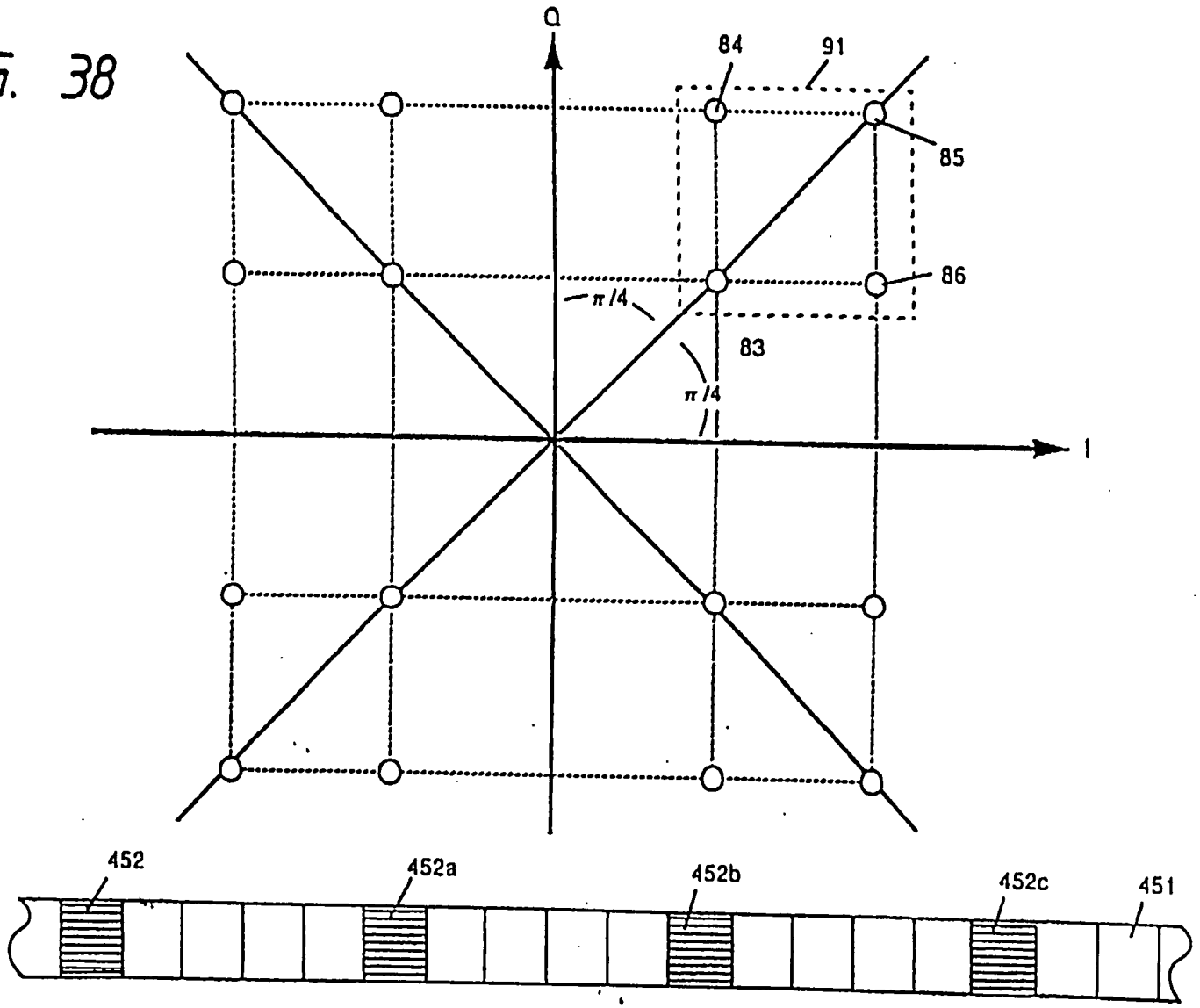


FIG. 39

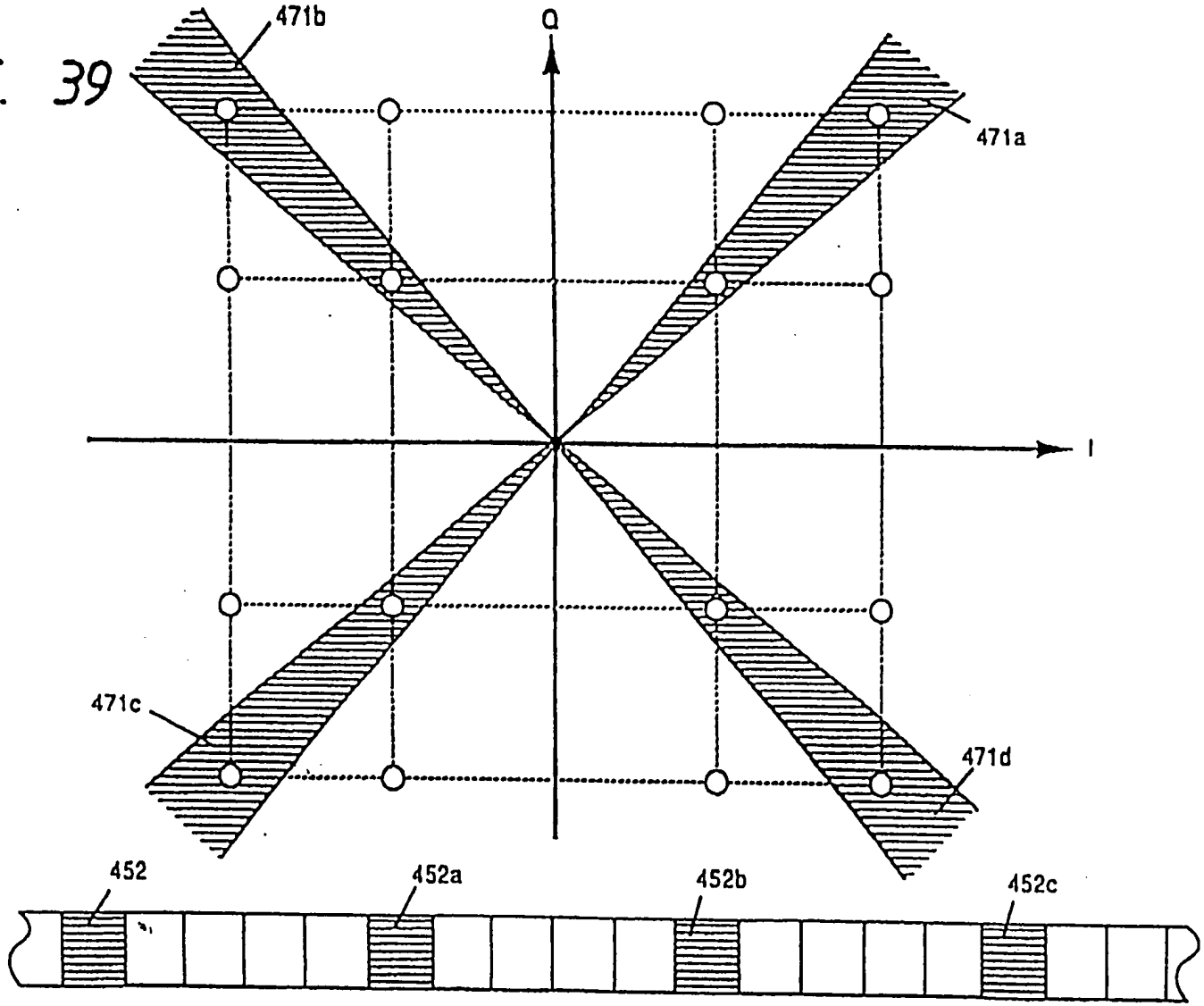


FIG. 40

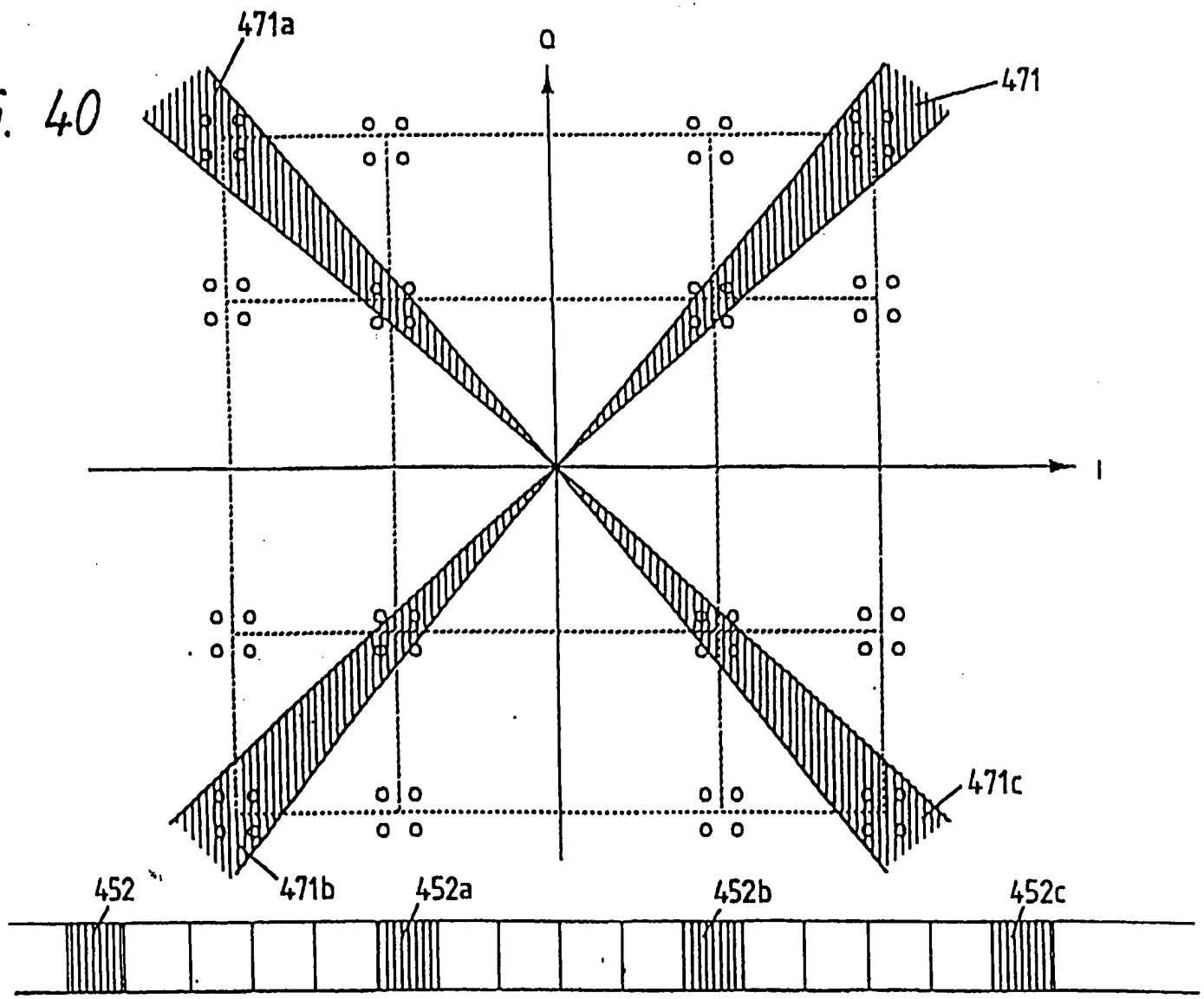


FIG. 41

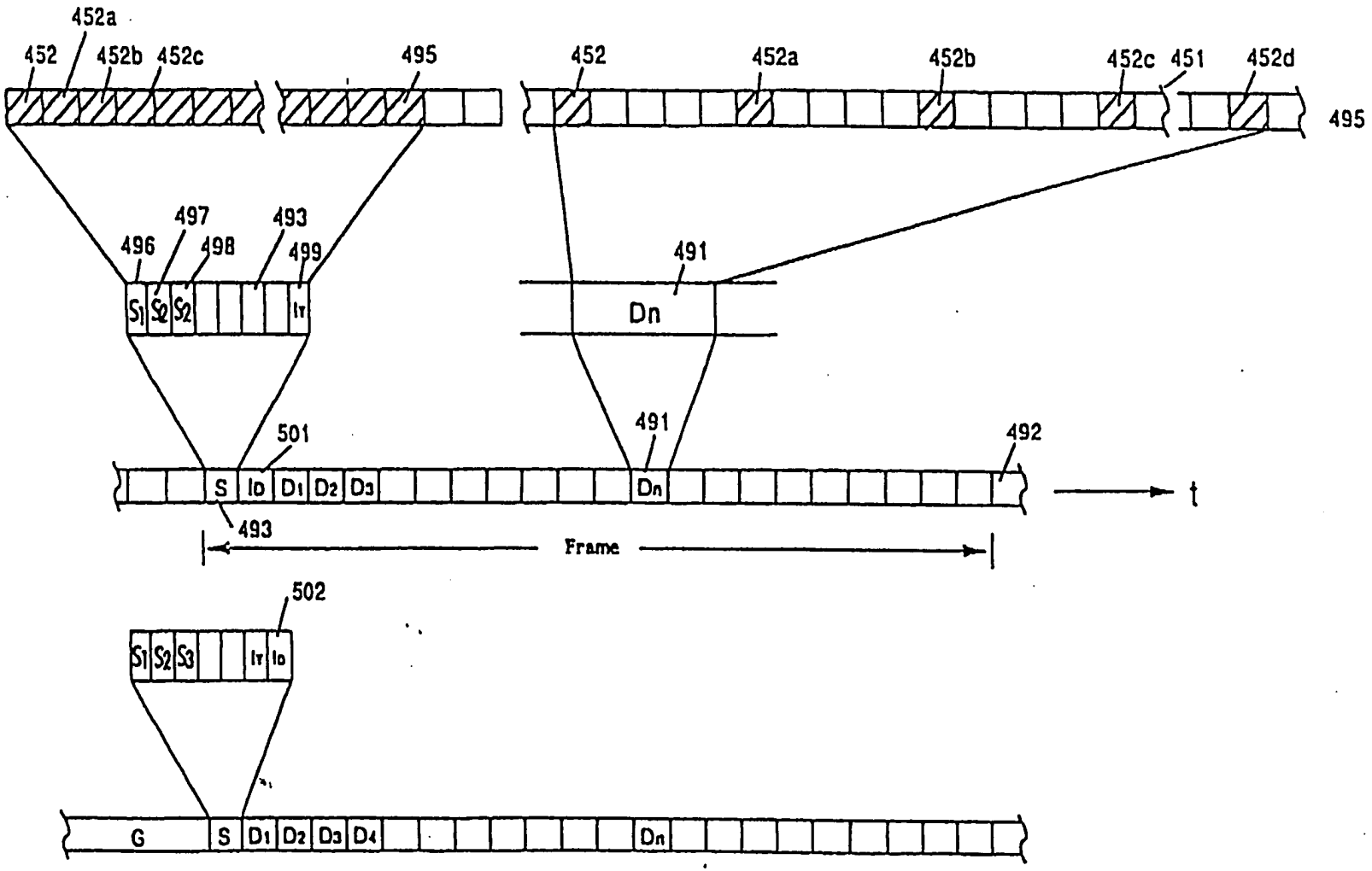

452a
452
452b
452c
495
452
452a
452b
452c
451
452d
495
497
493
496
498
499
491
S1
S2
S2
IT
Dn
501
491
492
S
ID
D1
D2
D3
Dn
t
493
Frame
502
S1
S2
S3
IT
ID
G
S
D1
D2
D3
D4
Dn

FIG. 42

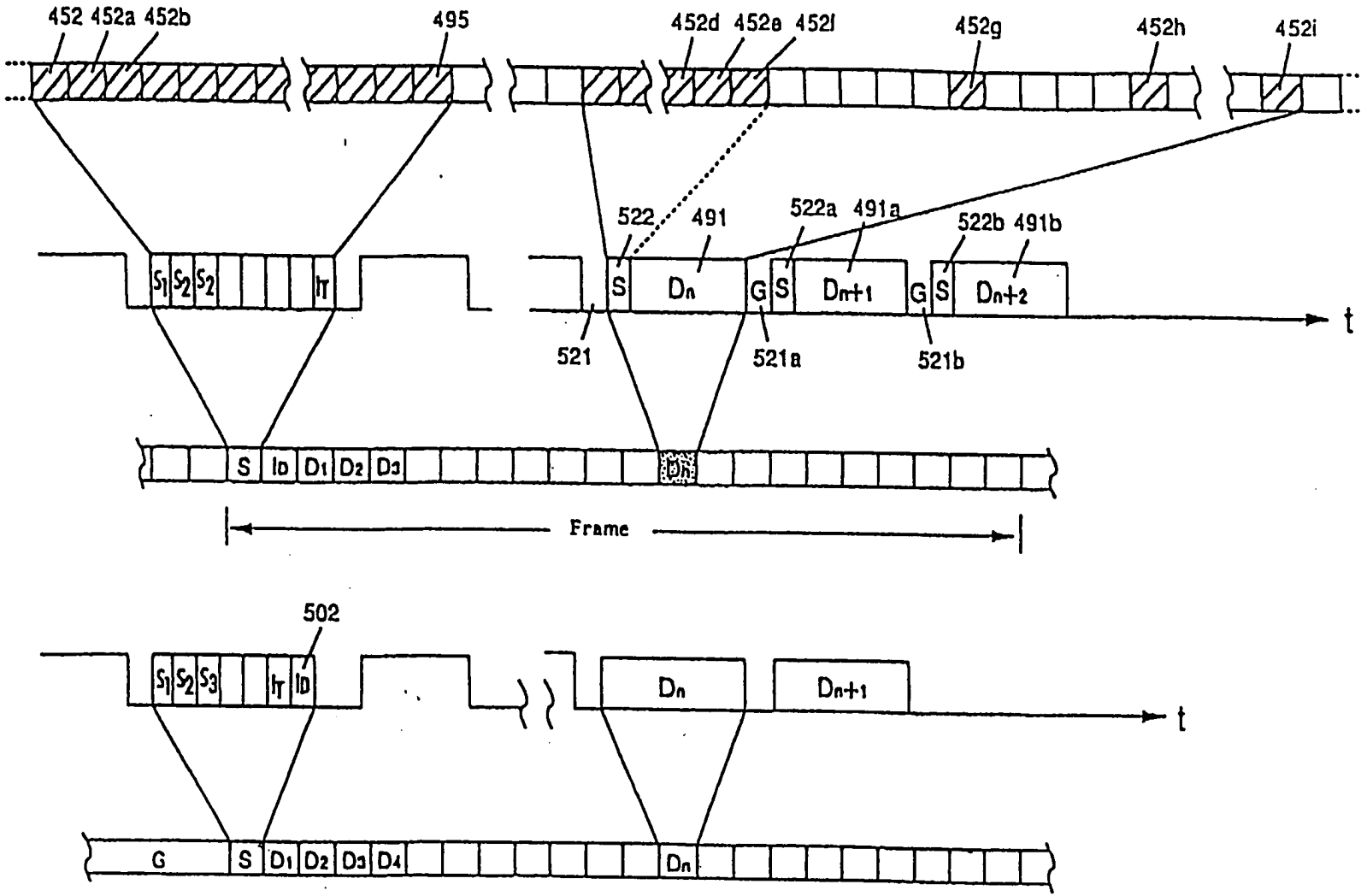

452 452a 452b
495
452d 452e 452l
452g
452h
452i
522
491
522a 491a
522b 491b
S1 S2 S2 IT
S Dn G S Dn+1 G S Dn+2
t
521
521a
521b
S ID D1 D2 D3
Dn
Frame
502
S1 S2 S3 IT ID
Dn
Dn+1
t
G S D1 D2 D3 D4
Dn

FIG. 43

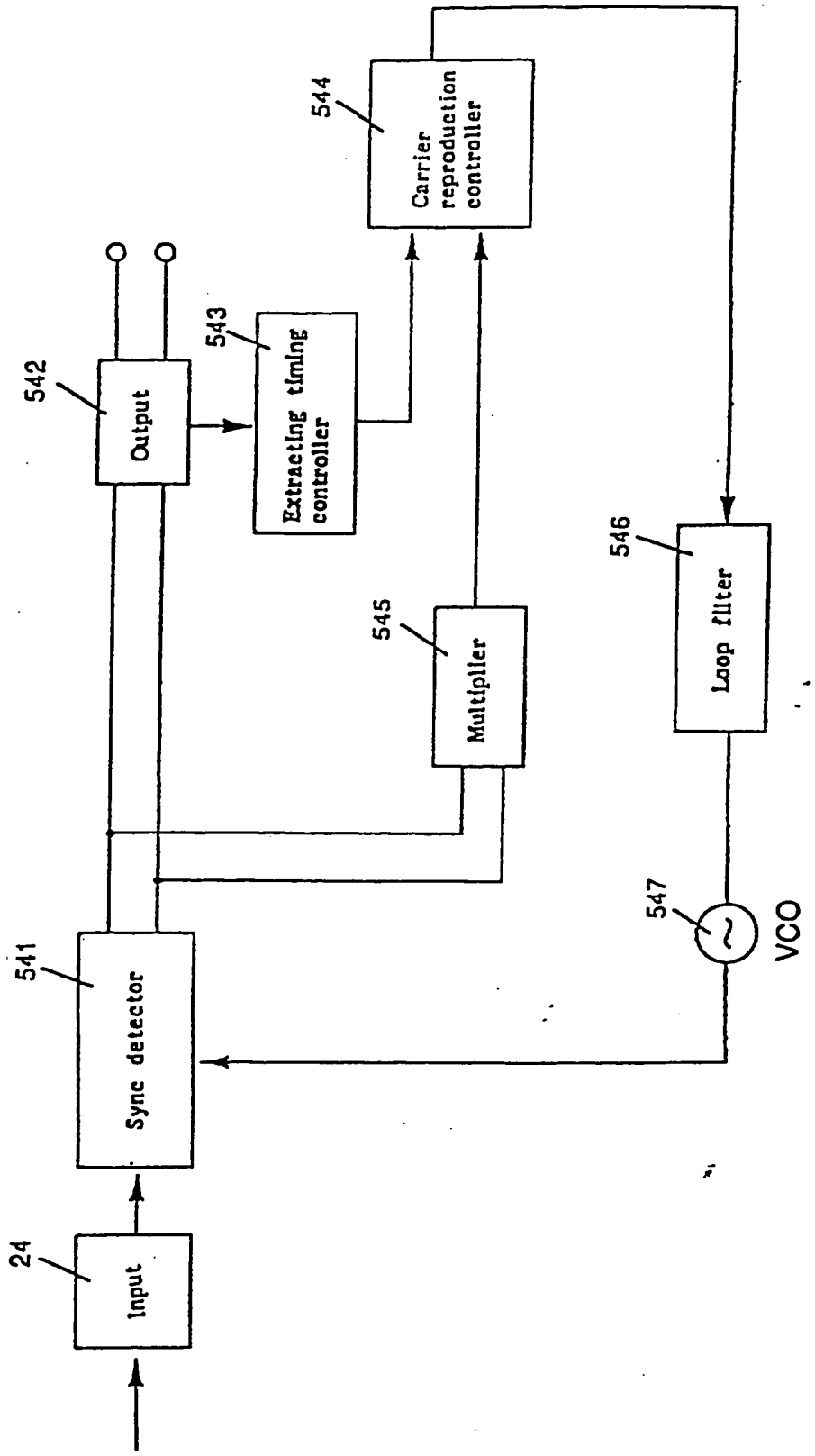
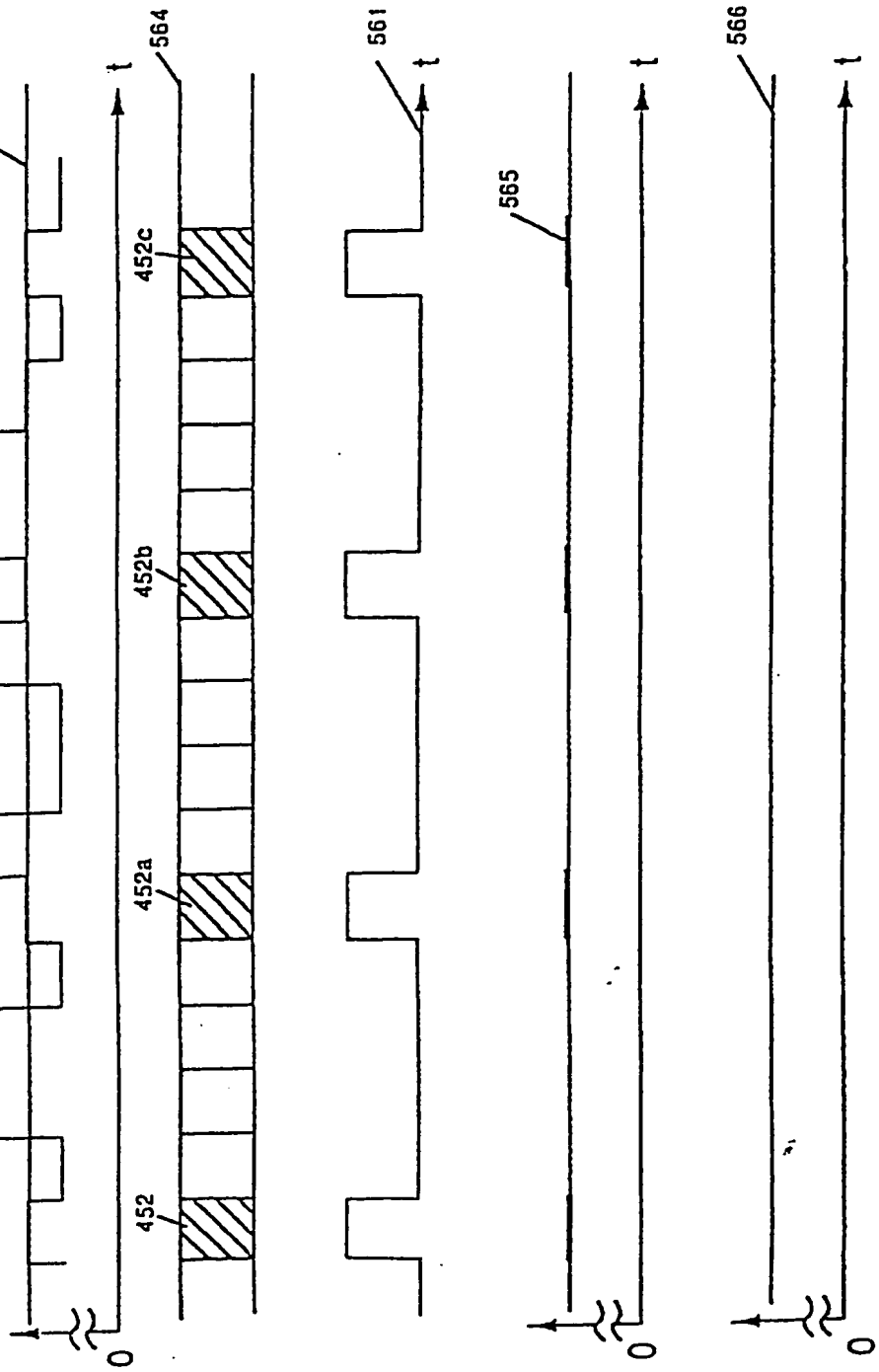

24
Input
541
Sync detector
542
Output
543
Extracting timing controller
544
Carrier reproduction controller
545
Multiplier
546
Loop filter
547
VCO

FIG. 44



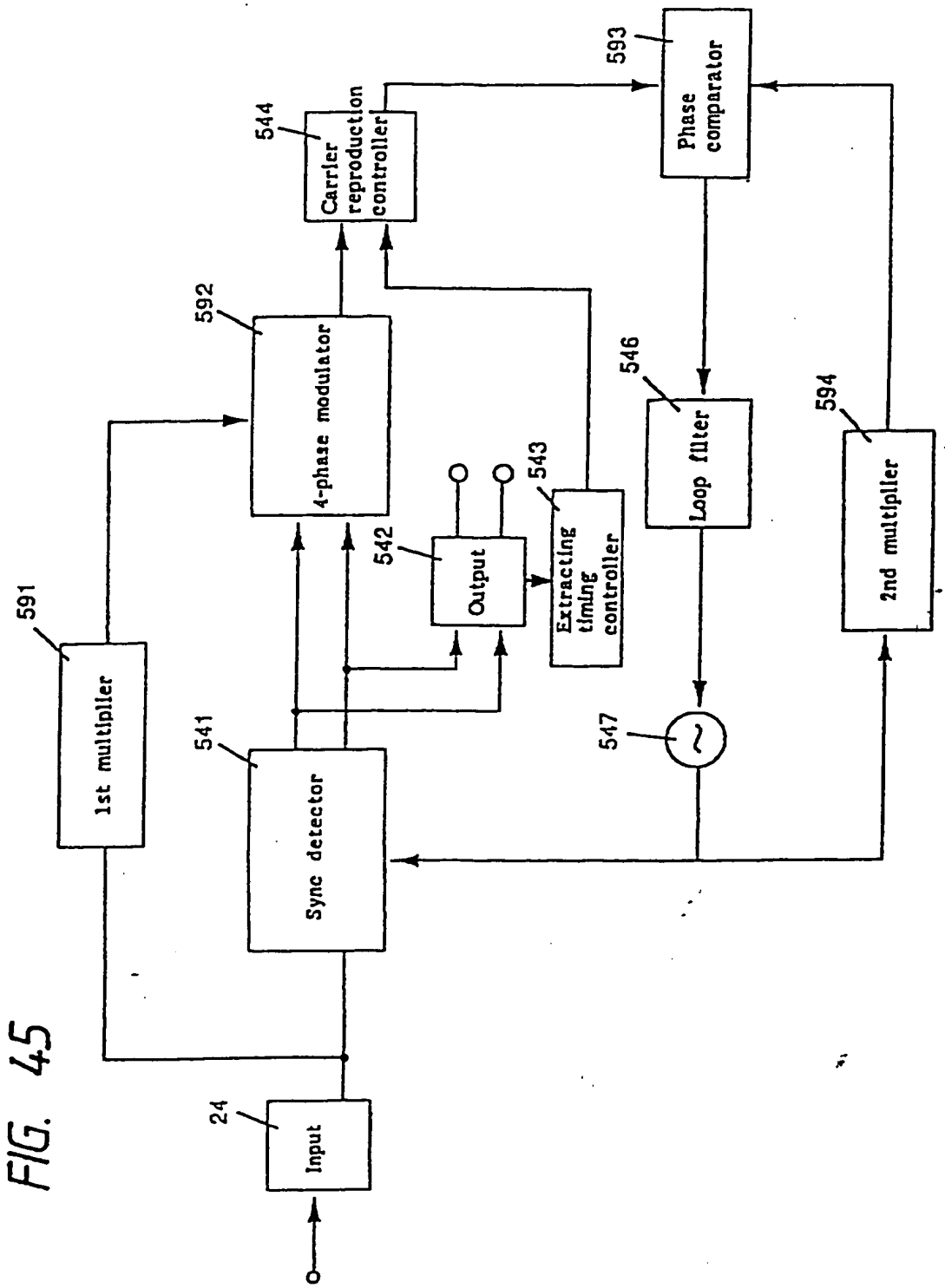

24
Input
591
1st multiplier
592
4-phase modulator
541
Sync detector
542
Output
543
Extracting timing controller
544
Carrier reproduction controller
593
Phase comparator
546
Loop filter
547
~
594
2nd multiplier

FIG. 45

FIG. 46

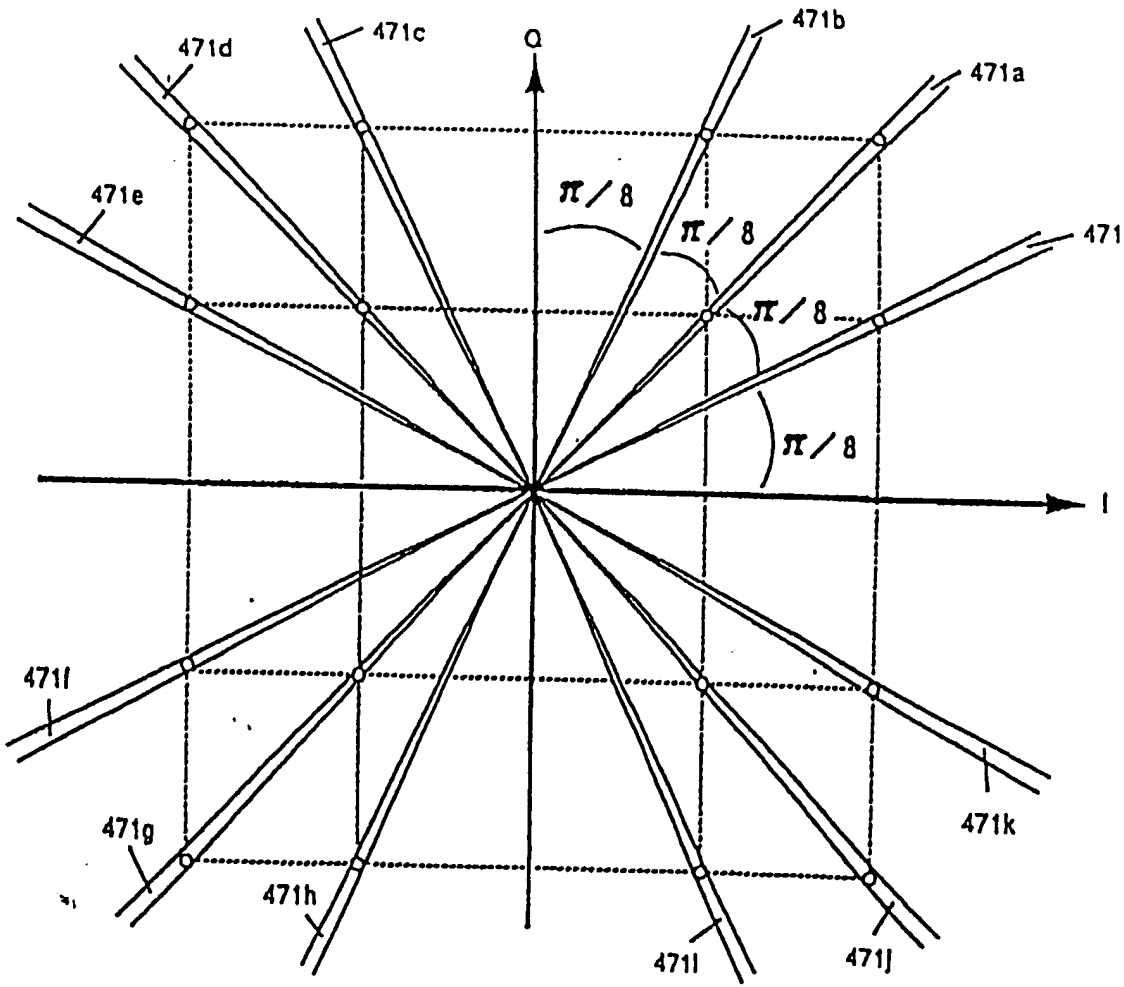

Q
I
471a
471b
471c
471d
471e
471
471f
471g
471h
471i
471j
471k
π / 8
π / 8
π / 8
π / 8

FIG. 47

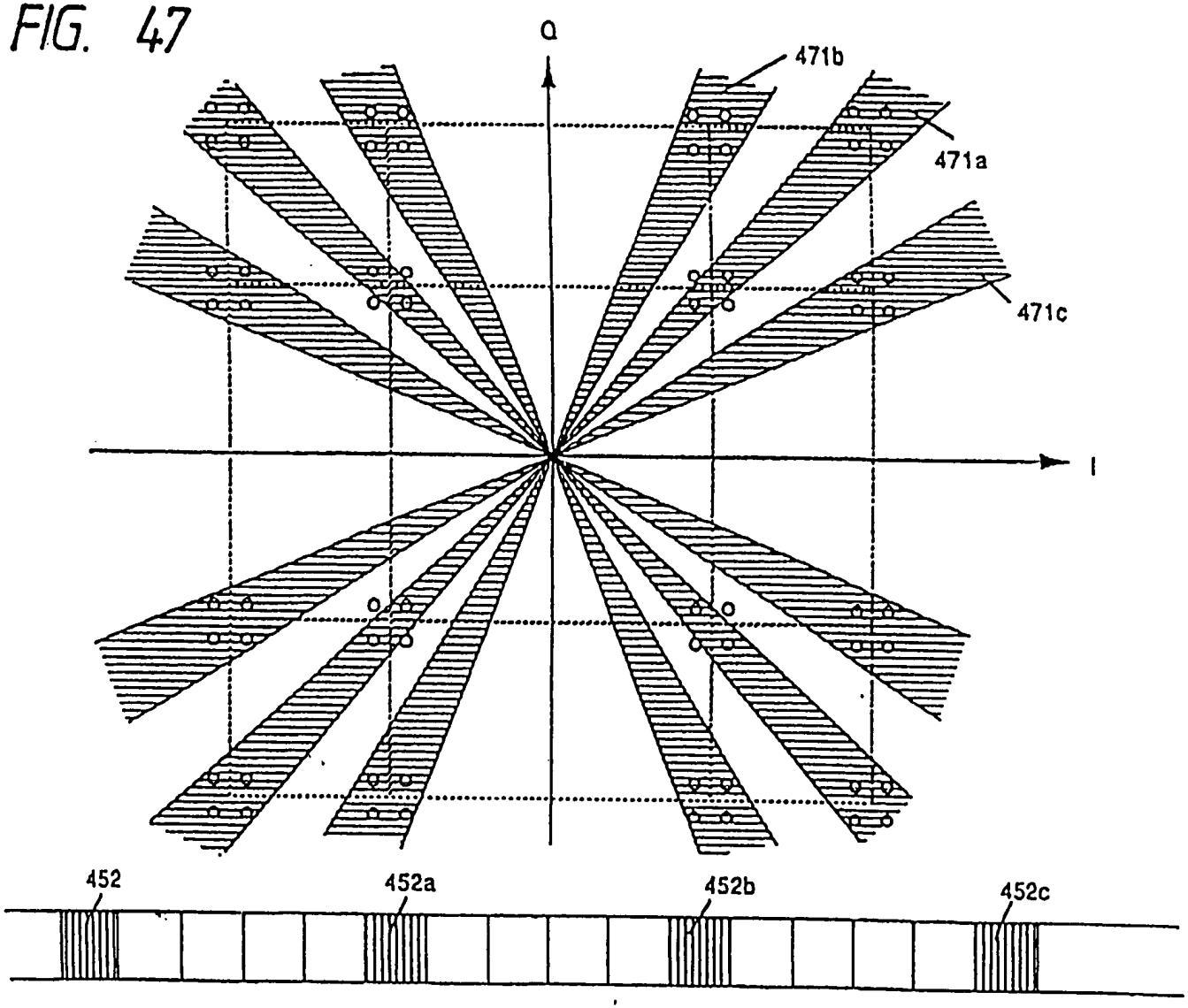


FIG. 48

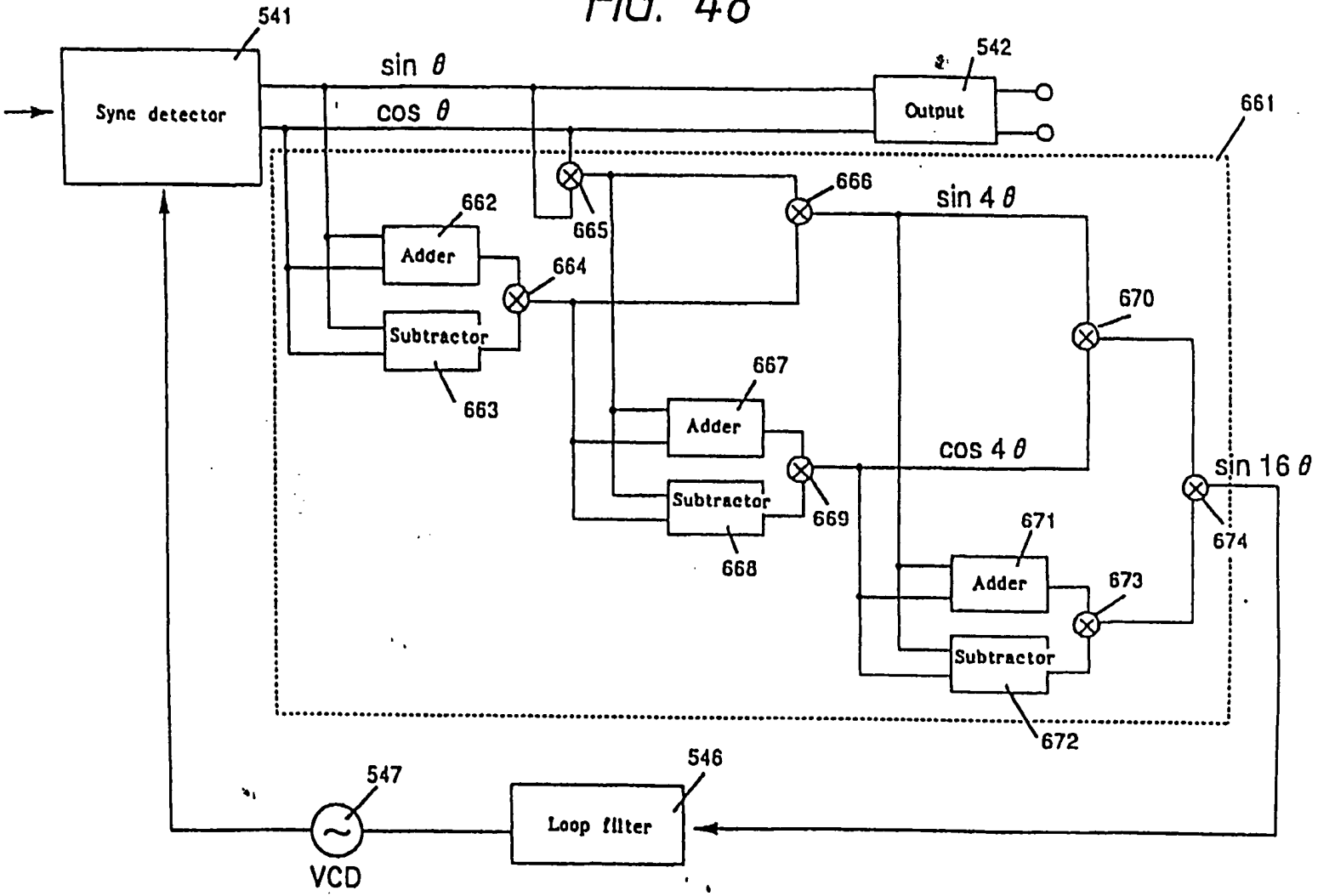

541
Sync detector
sin θ
cos θ
542
Output
661
662
Adder
665
666
sin 4 θ
664
Subtractor
663
670
667
Adder
cos 4 θ
sin 16 θ
669
Subtractor
668
671
Adder
673
674
Subtractor
672
547
546
Loop filter
VCD

FIG. 49

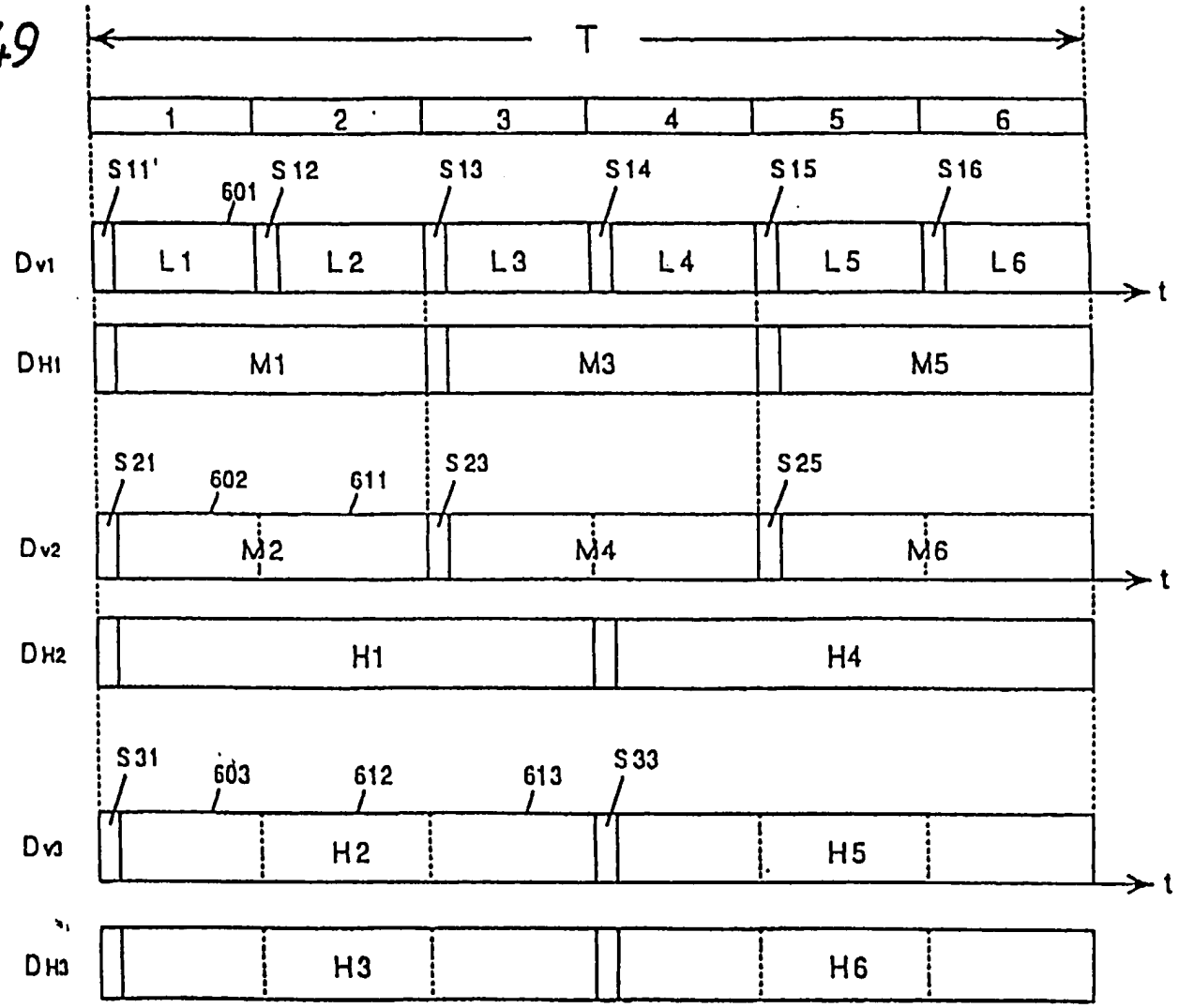

T
1
2
3
4
5
6
S11'
601
S12
S13
S14
S15
S16
Dv1
L1
L2
L3
L4
L5
L6
t
DH1
M1
M3
M5
S21
602
611
S23
S25
Dv2
M2
M4
M6
t
DH2
H1
H4
S31
603
612
613
S33
Dv3
H2
H5
t
DH3
H3
H6

FIG. 50

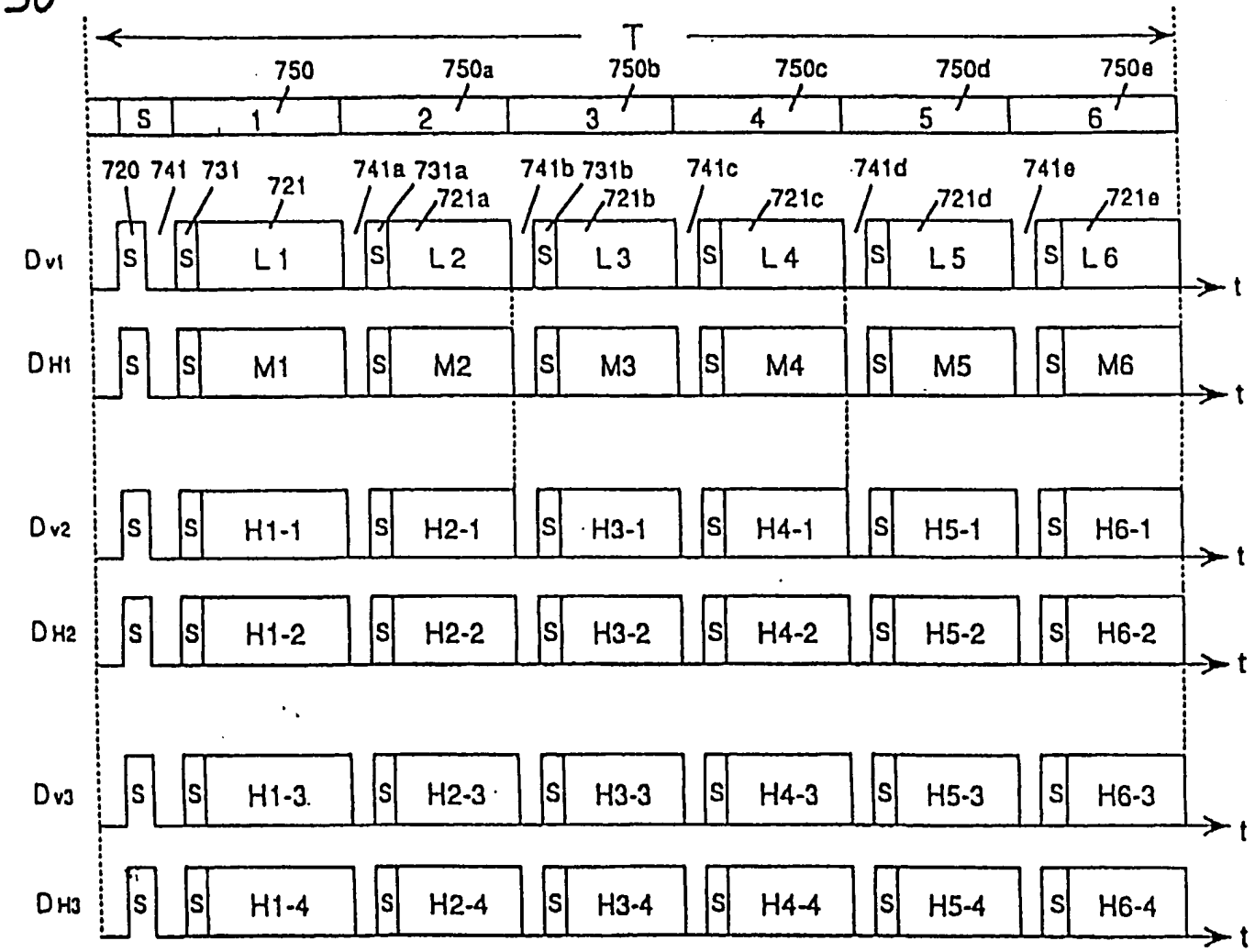

T
750
750a
750b
750c
750d
750e
S
1
2
3
4
5
6
720
741
731
721
741a
731a
721a
741b
731b
721b
741c
721c
741d
721d
741e
721e
Dv1
L1
L2
L3
L4
L5
L6
DH1
M1
M2
M3
M4
M5
M6
Dv2
H1-1
H2-1
H3-1
H4-1
H5-1
H6-1
DH2
H1-2
H2-2
H3-2
H4-2
H5-2
H6-2
Dv3
H1-3
H2-3
H3-3
H4-3
H5-3
H6-3
DH3
H1-4
H2-4
H3-4
H4-4
H5-4
H6-4
t

FIG. 51

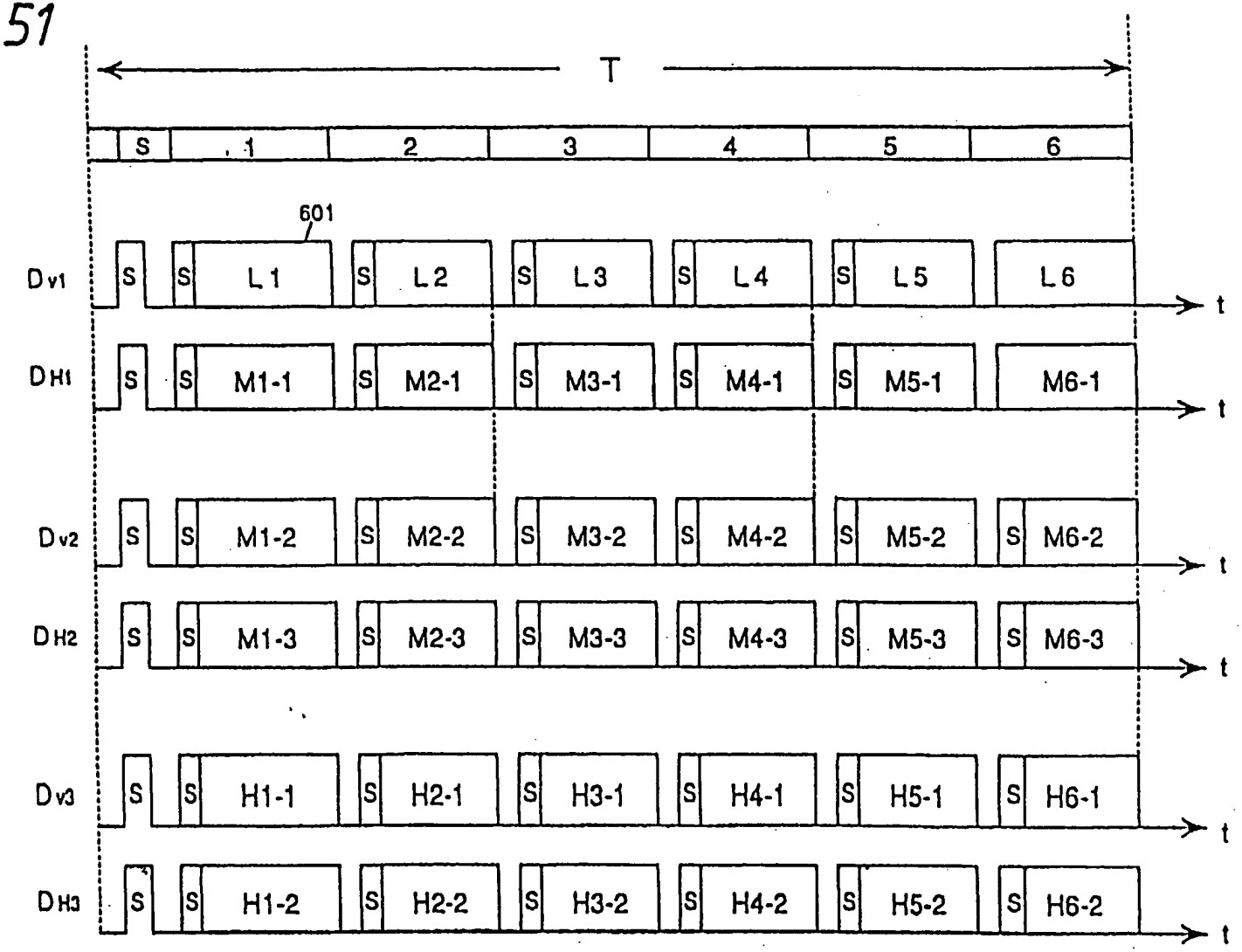

T
S
1
2
3
4
5
6
601
DV1
DH1
DV2
DH2
DV3
DH3
L1
L2
L3
L4
L5
L6
M1-1
M2-1
M3-1
M4-1
M5-1
M6-1
M1-2
M2-2
M3-2
M4-2
M5-2
M6-2
M1-3
M2-3
M3-3
M4-3
M5-3
M6-3
H1-1
H2-1
H3-1
H4-1
H5-1
H6-1
H1-2
H2-2
H3-2
H4-2
H5-2
H6-2
t

FIG. 52

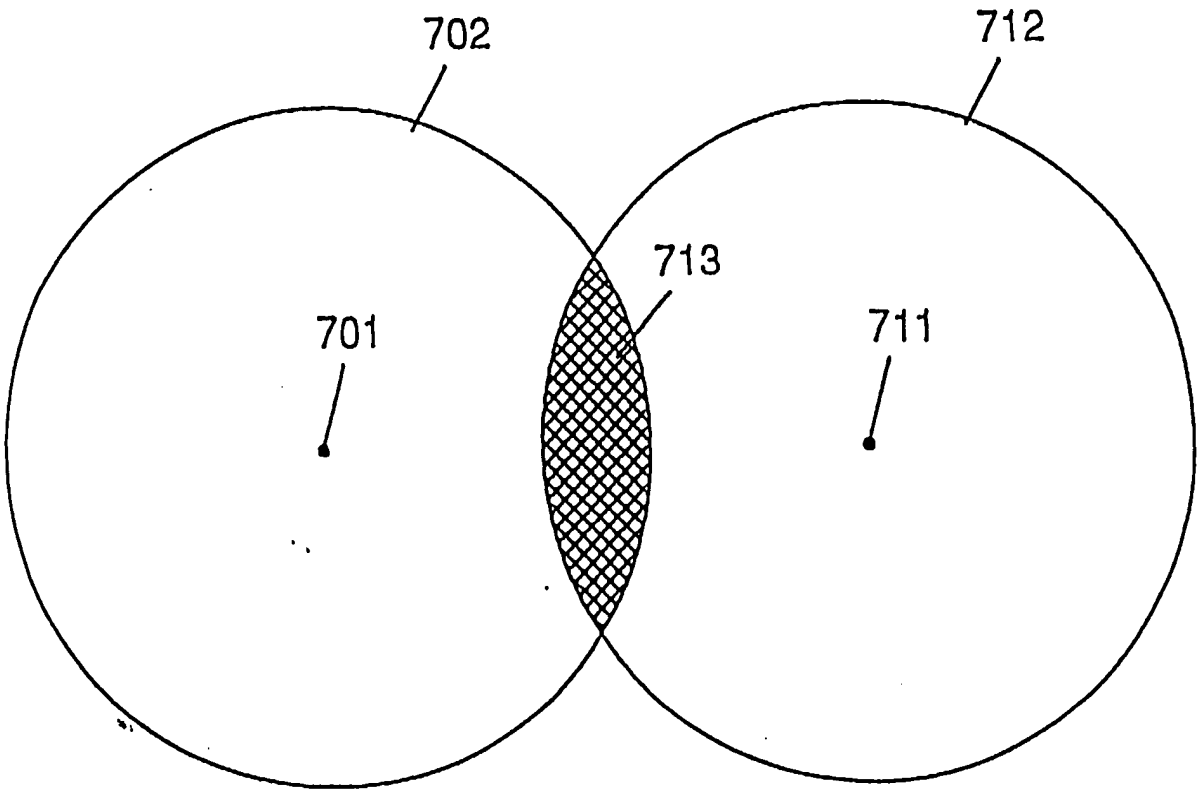


FIG. 53

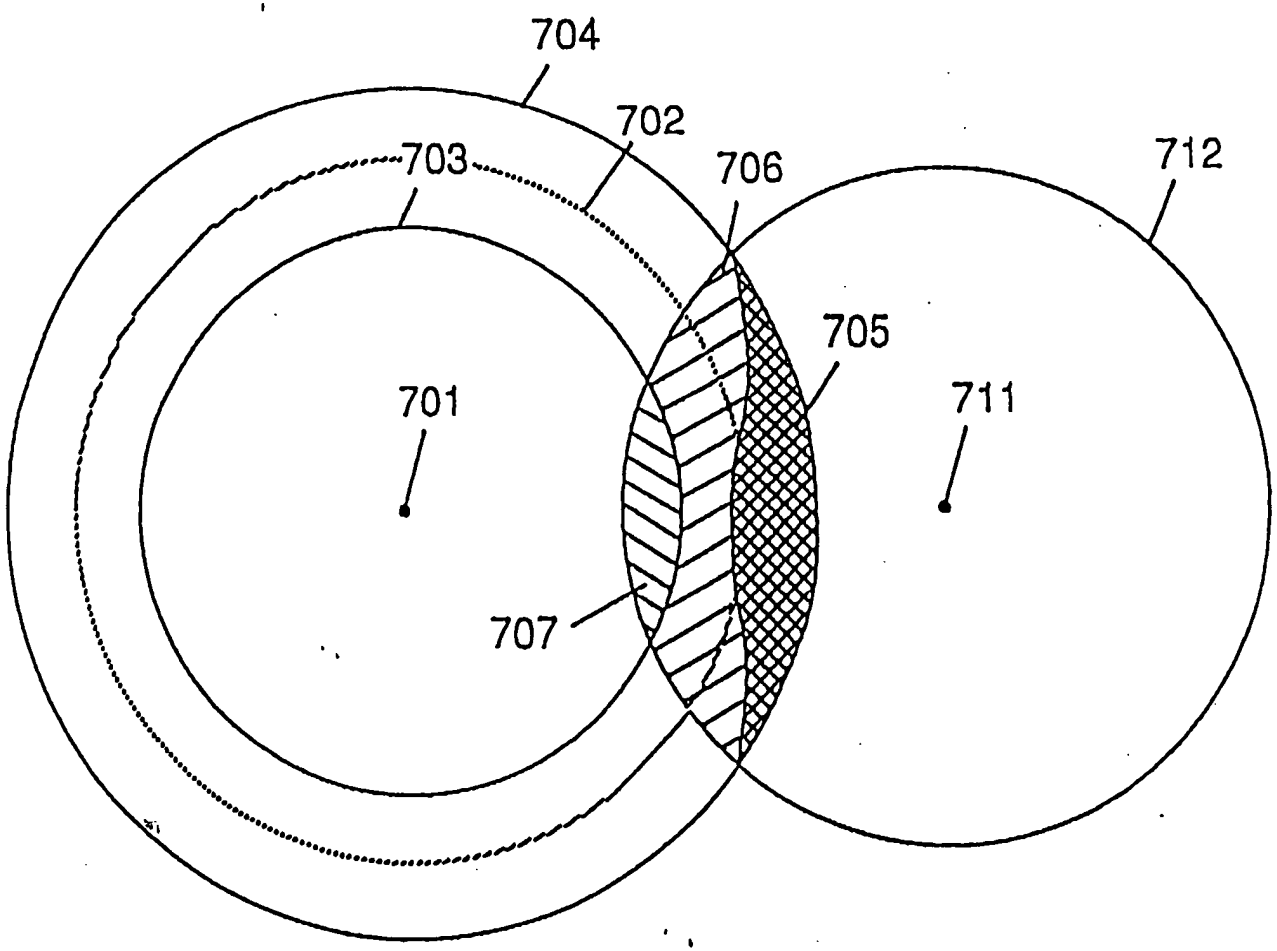


FIG. 54

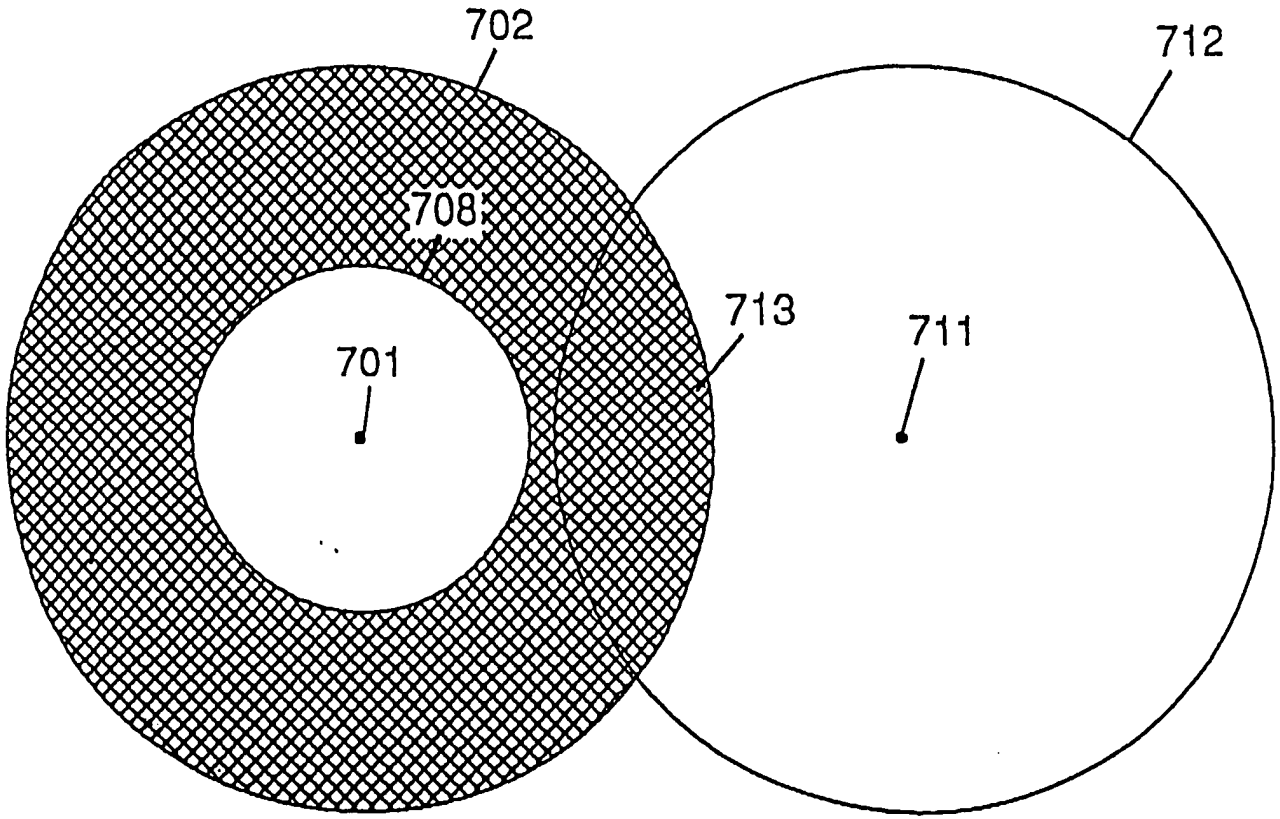


FIG. 55

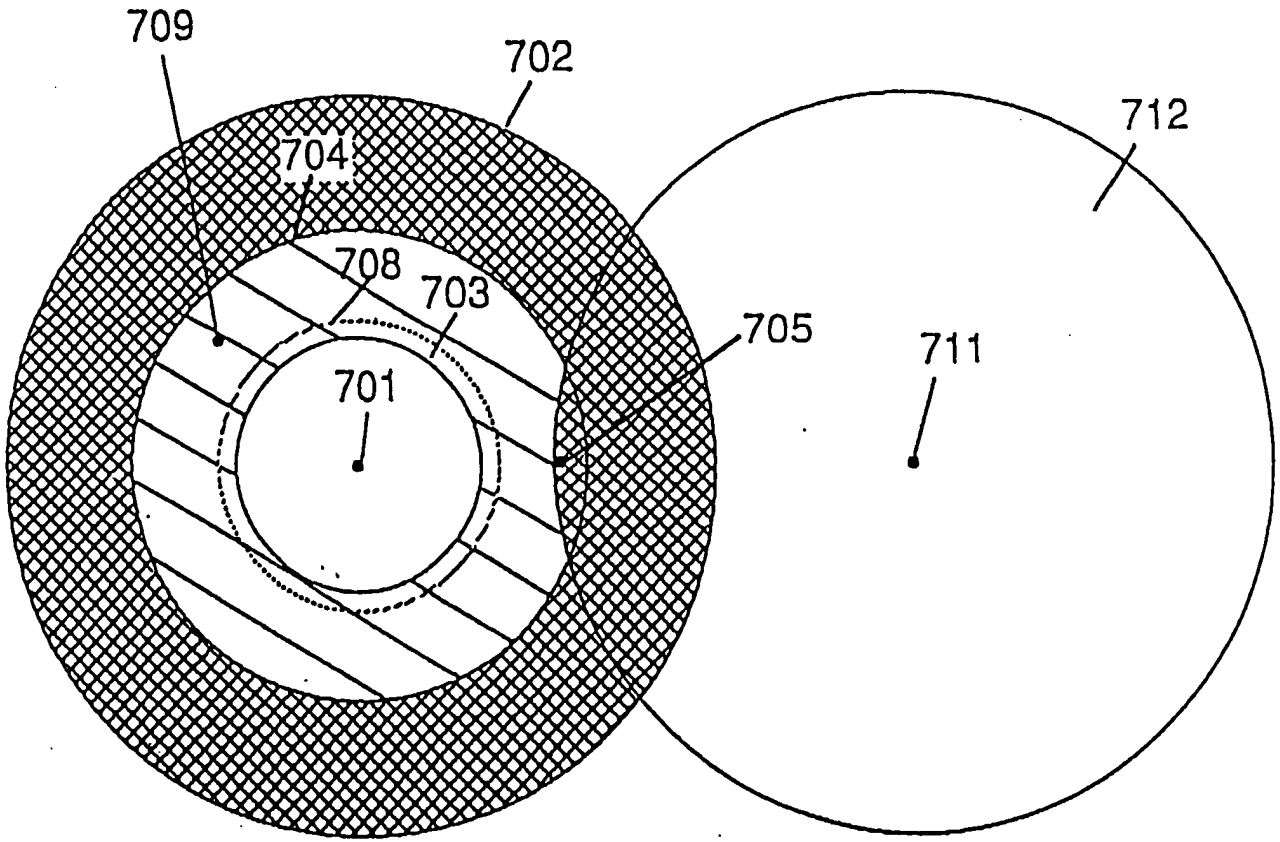


FIG. 56

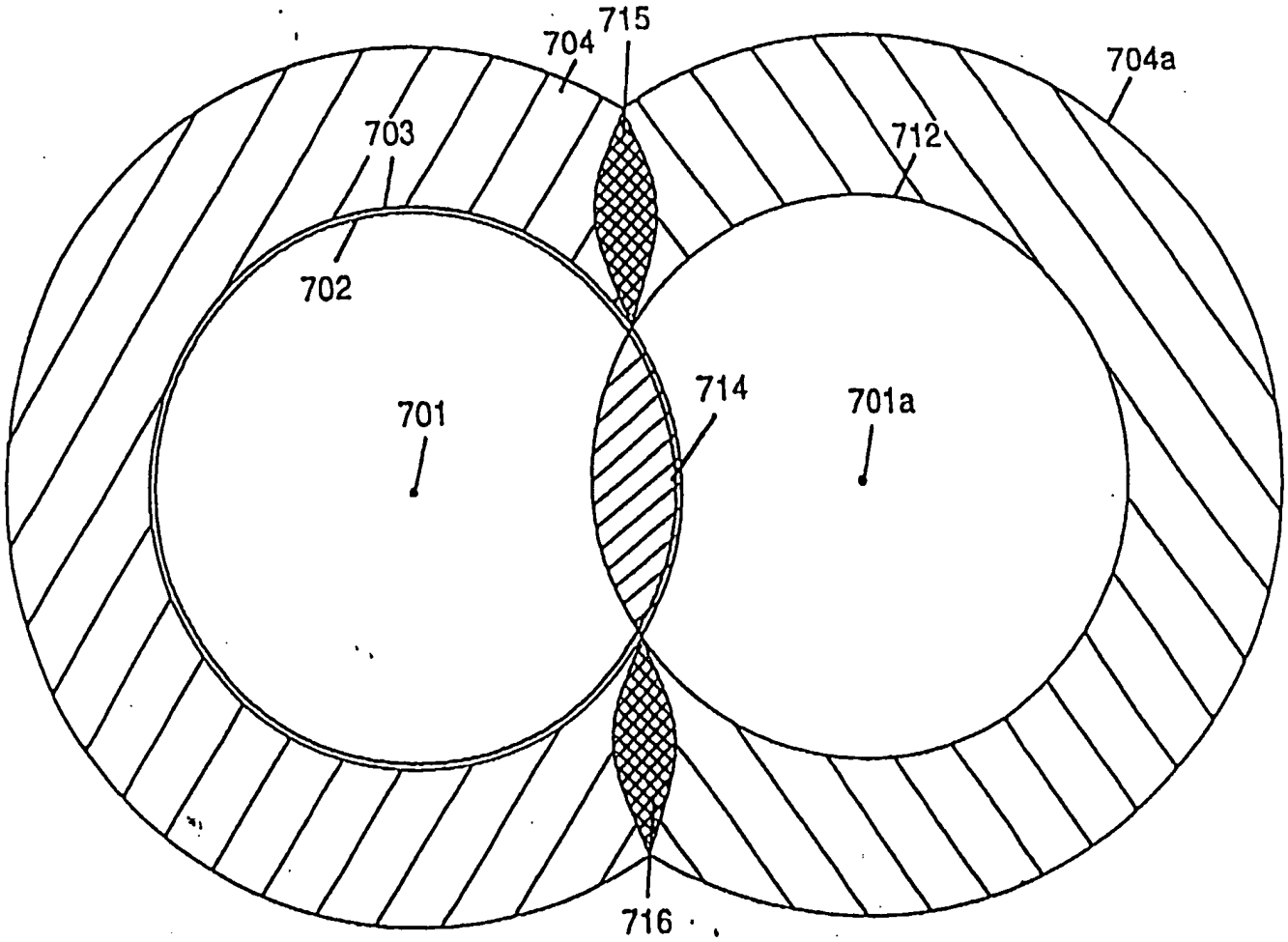


FIG. 57

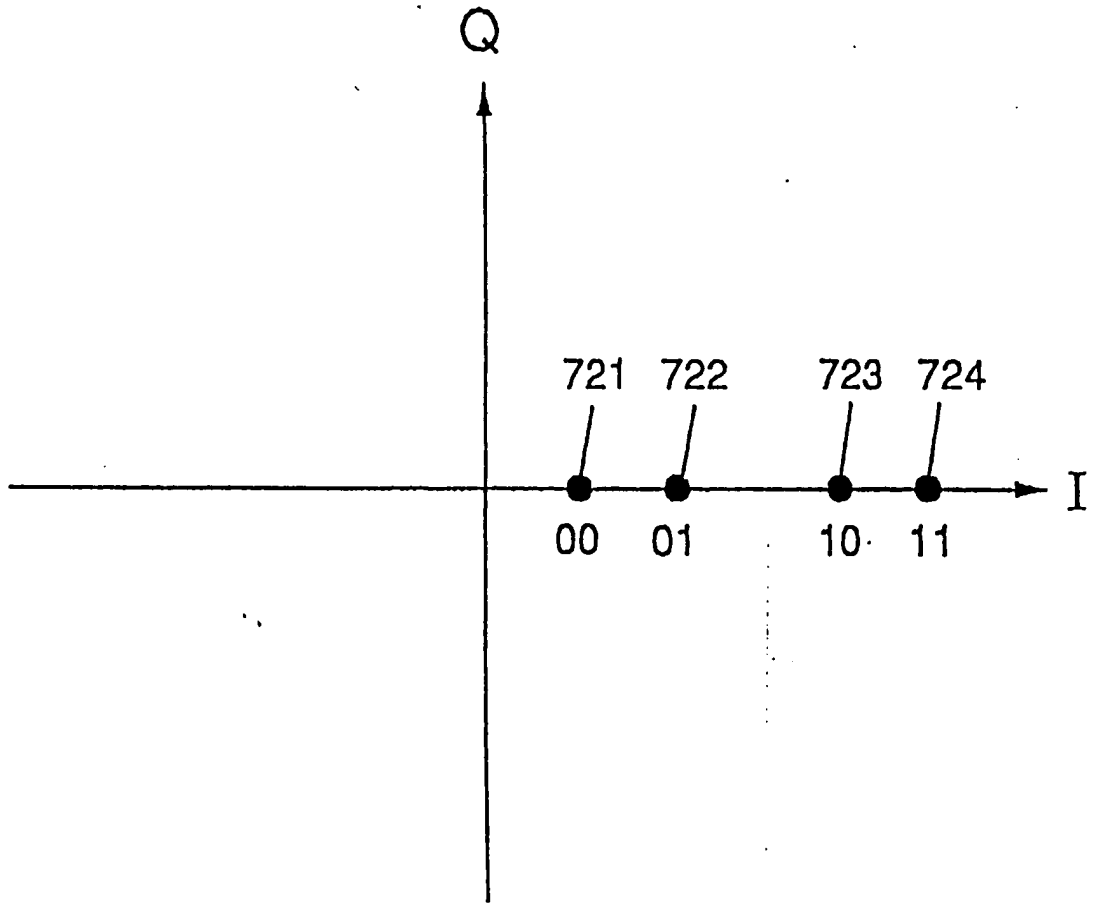


FIG. 58

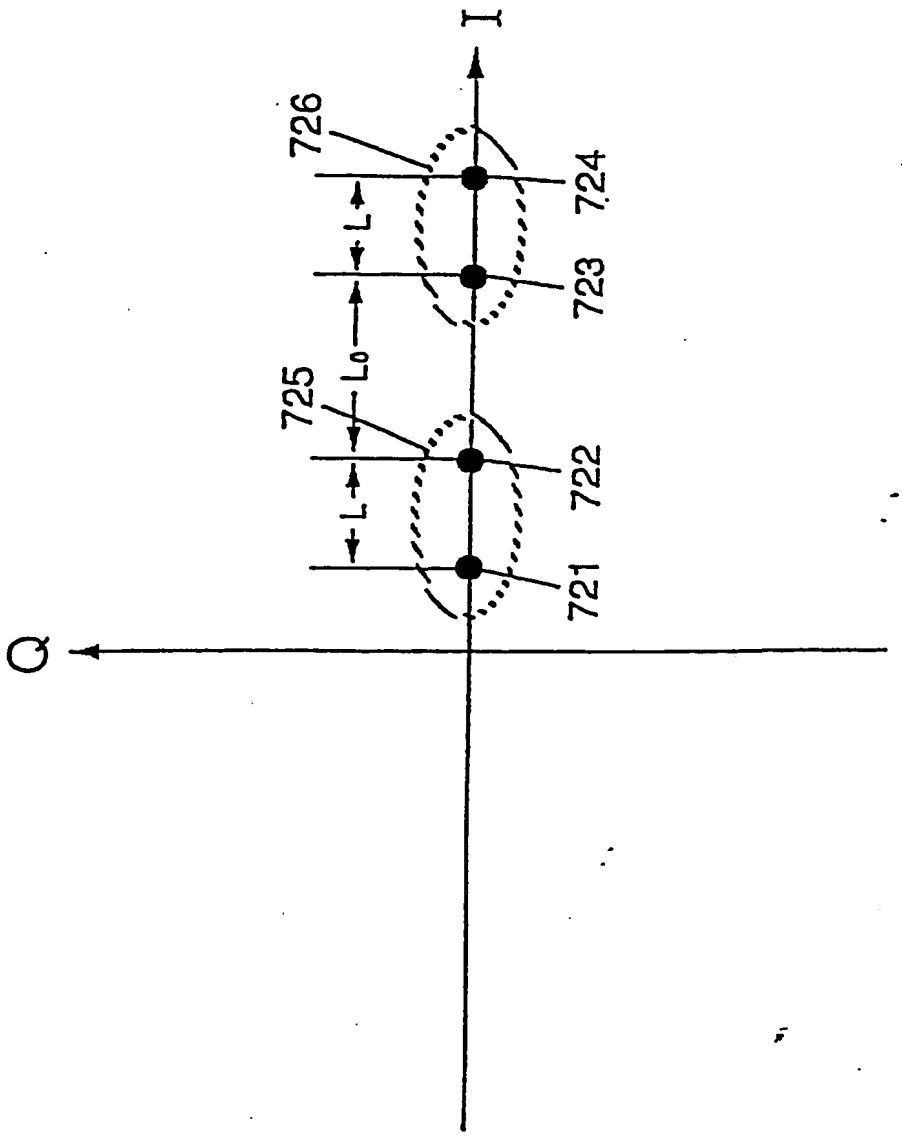


FIG. 59(a)

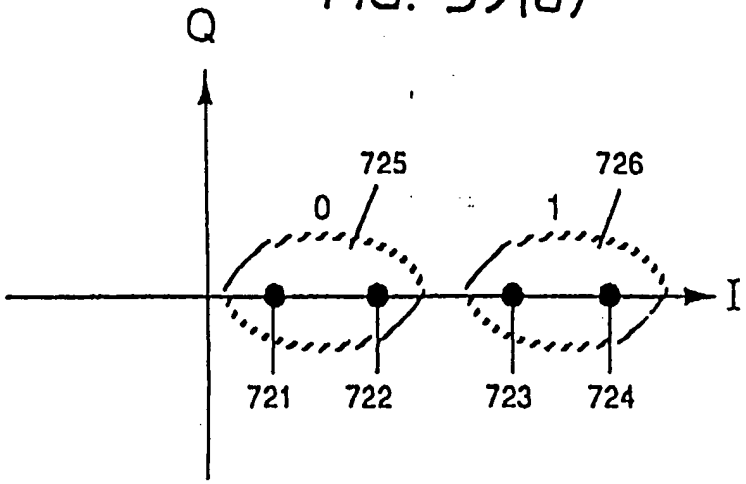


FIG. 59(b)

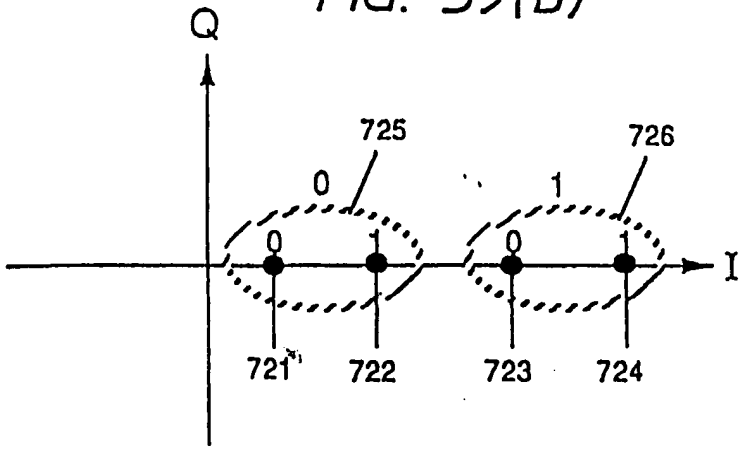


FIG. 59(c)

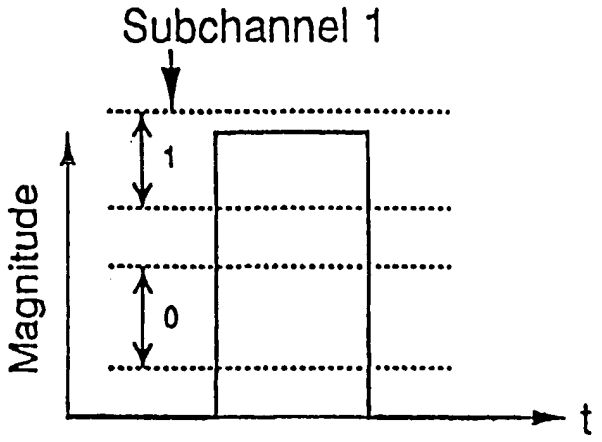


FIG. 59(d)

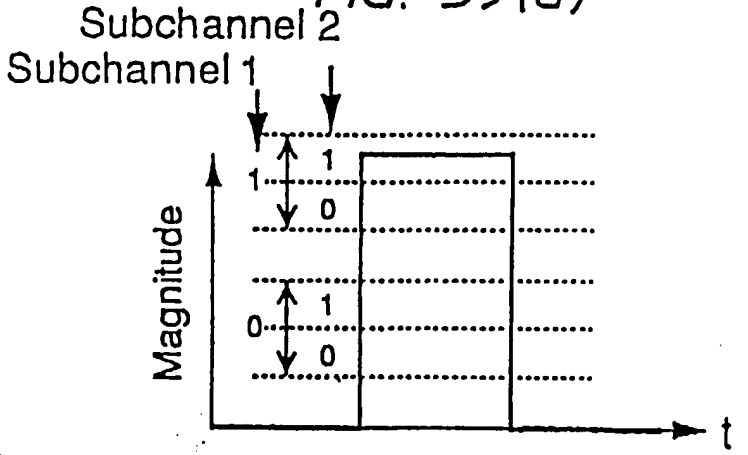


FIG. 60

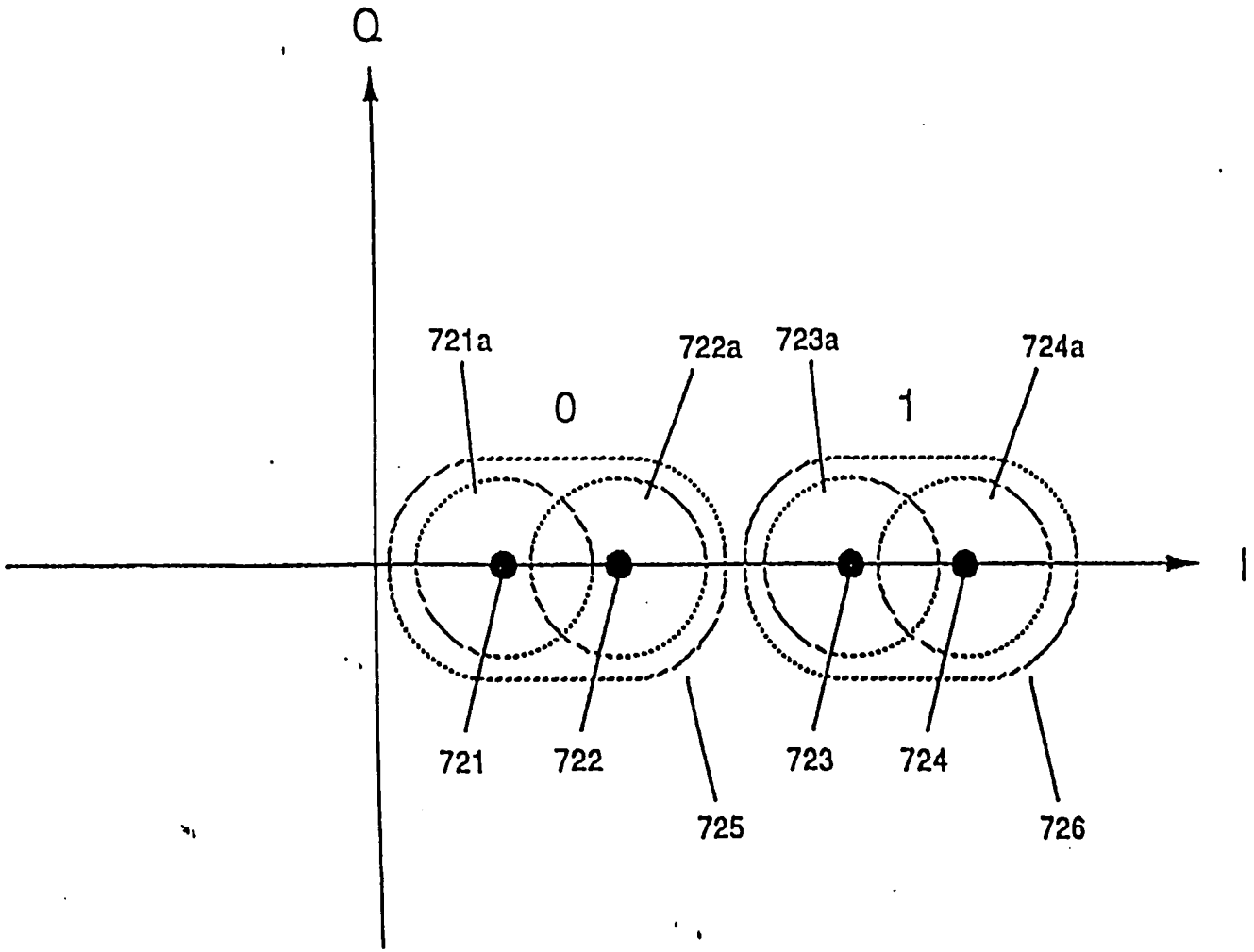


FIG. 61

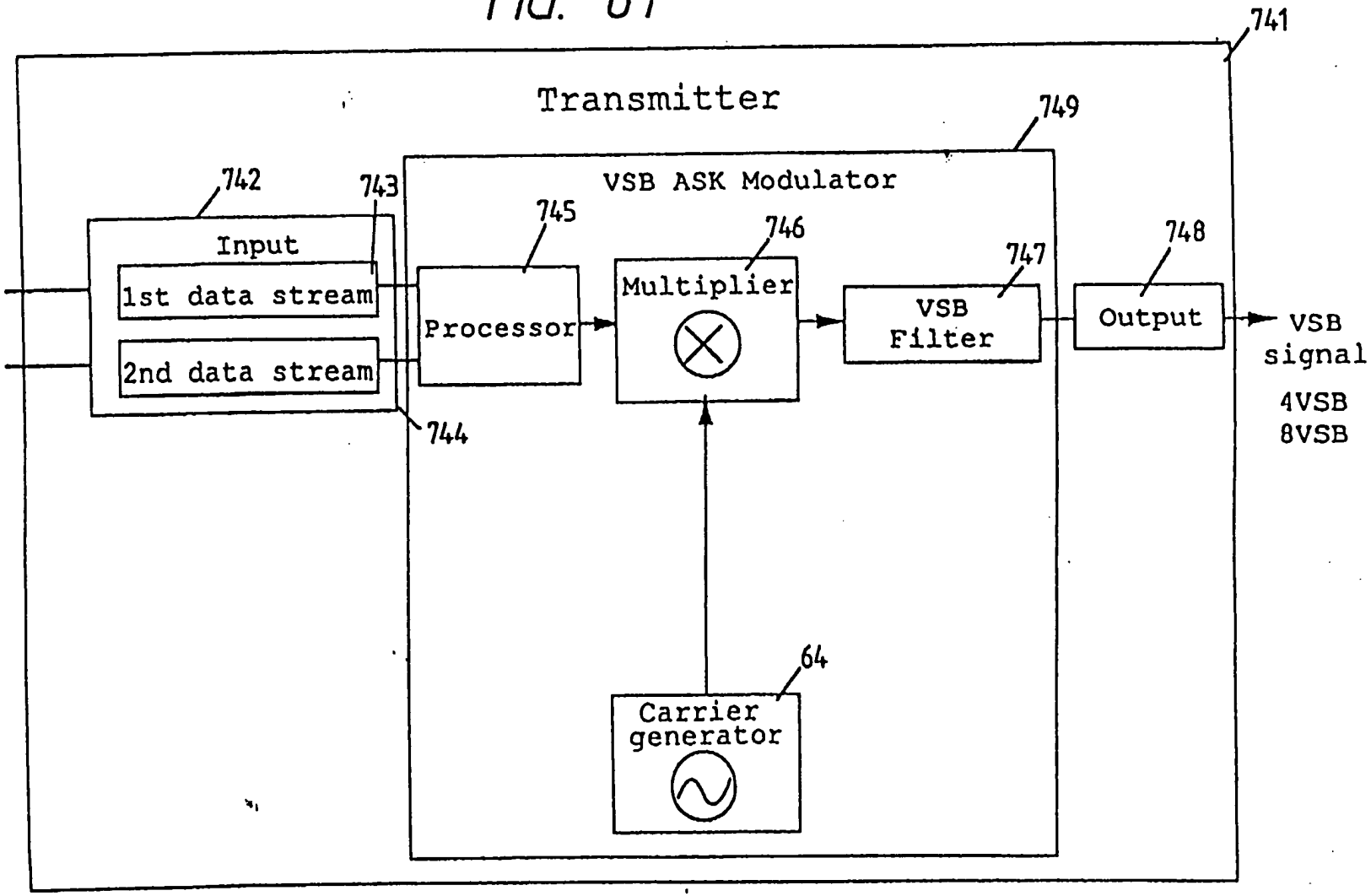

741
Transmitter
749
VSB ASK Modulator
742
743
Input
1st data stream
2nd data stream
744
745
Processor
746
Multiplier
747
VSB
Filter
748
Output
VSB
signal
4VSB
8VSB
64
Carrier
generator

FIG. 62(a)

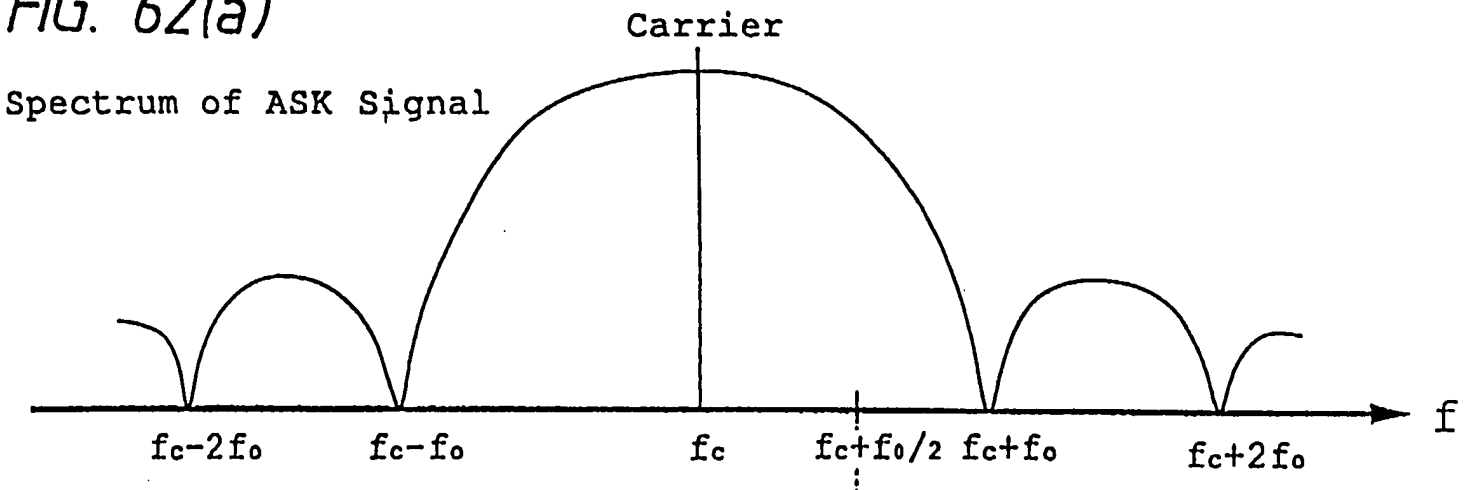


FIG. 62(b)

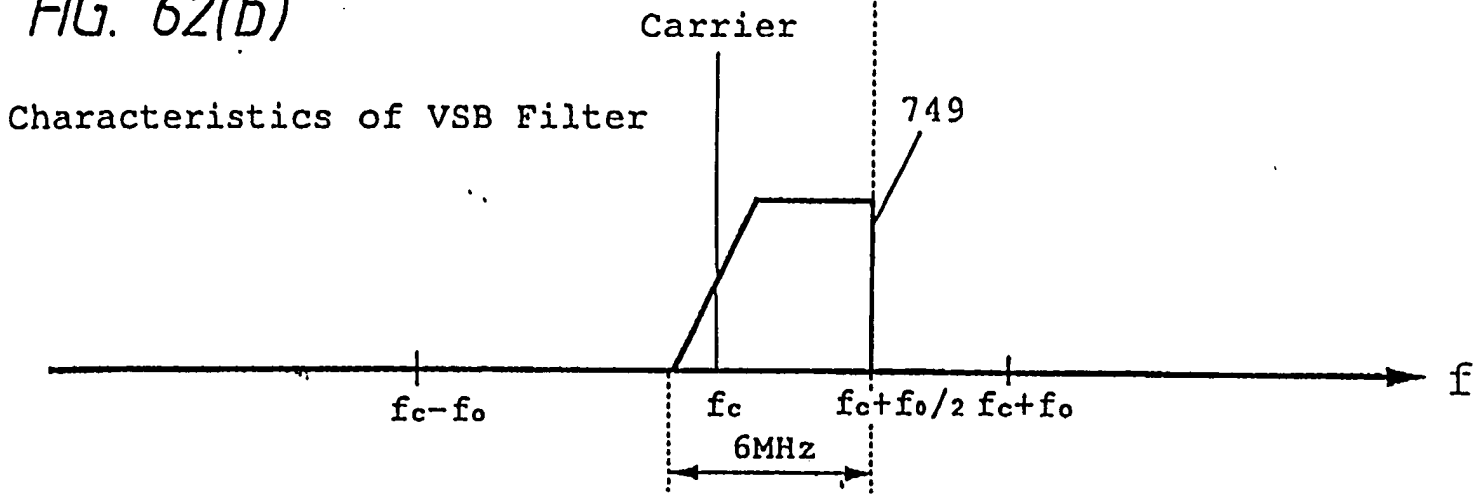


FIG. 63

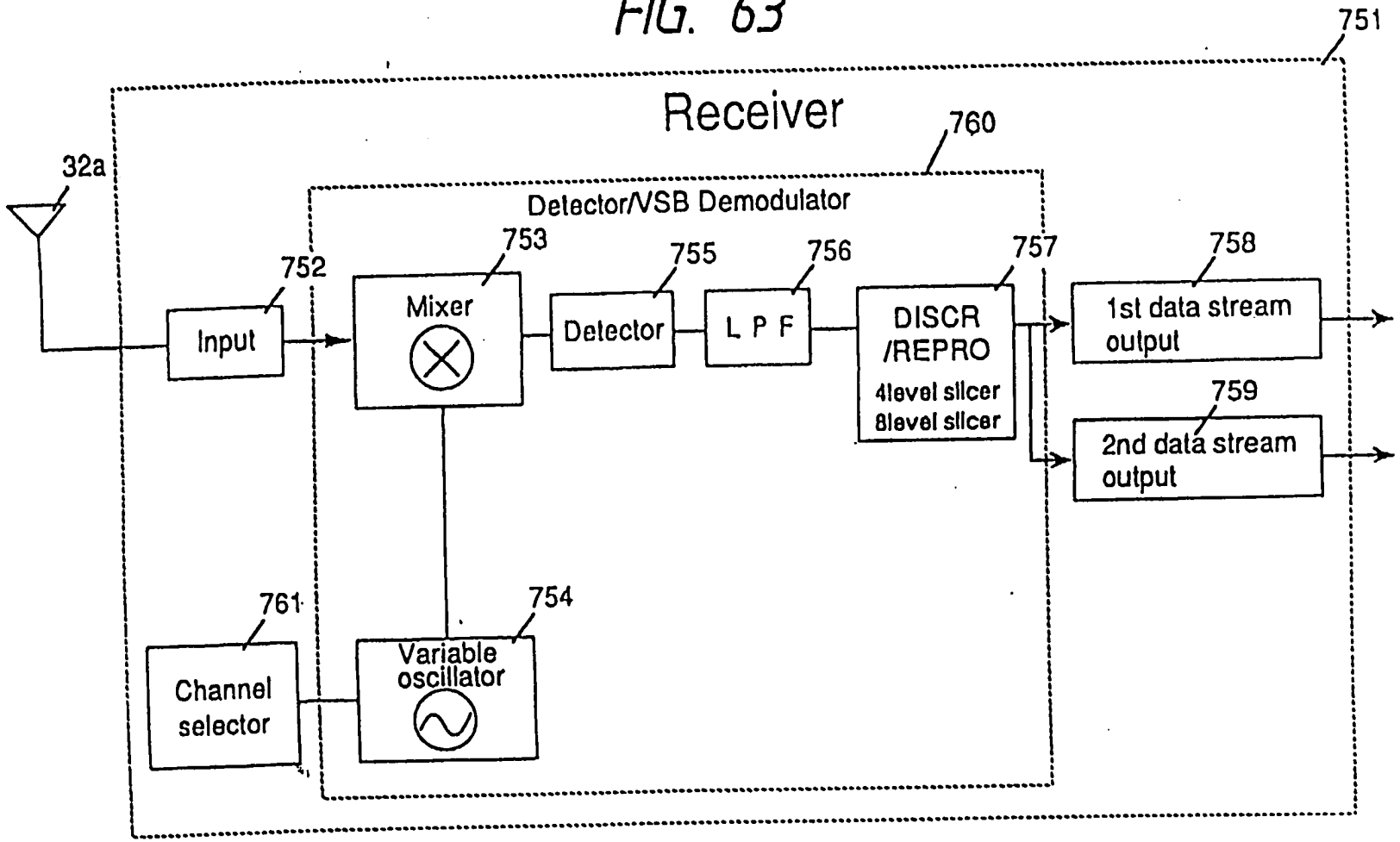

751
Receiver
760
32a
Detector/VSB Demodulator
752
753
755
756
757
758
Input
Mixer
Detector
L P F
DISCR
/REPRO
4level slicer
8level slicer
1st data stream
output
759
2nd data stream
output
761
754
Channel
selector
Variable
oscillator

FIG. 64

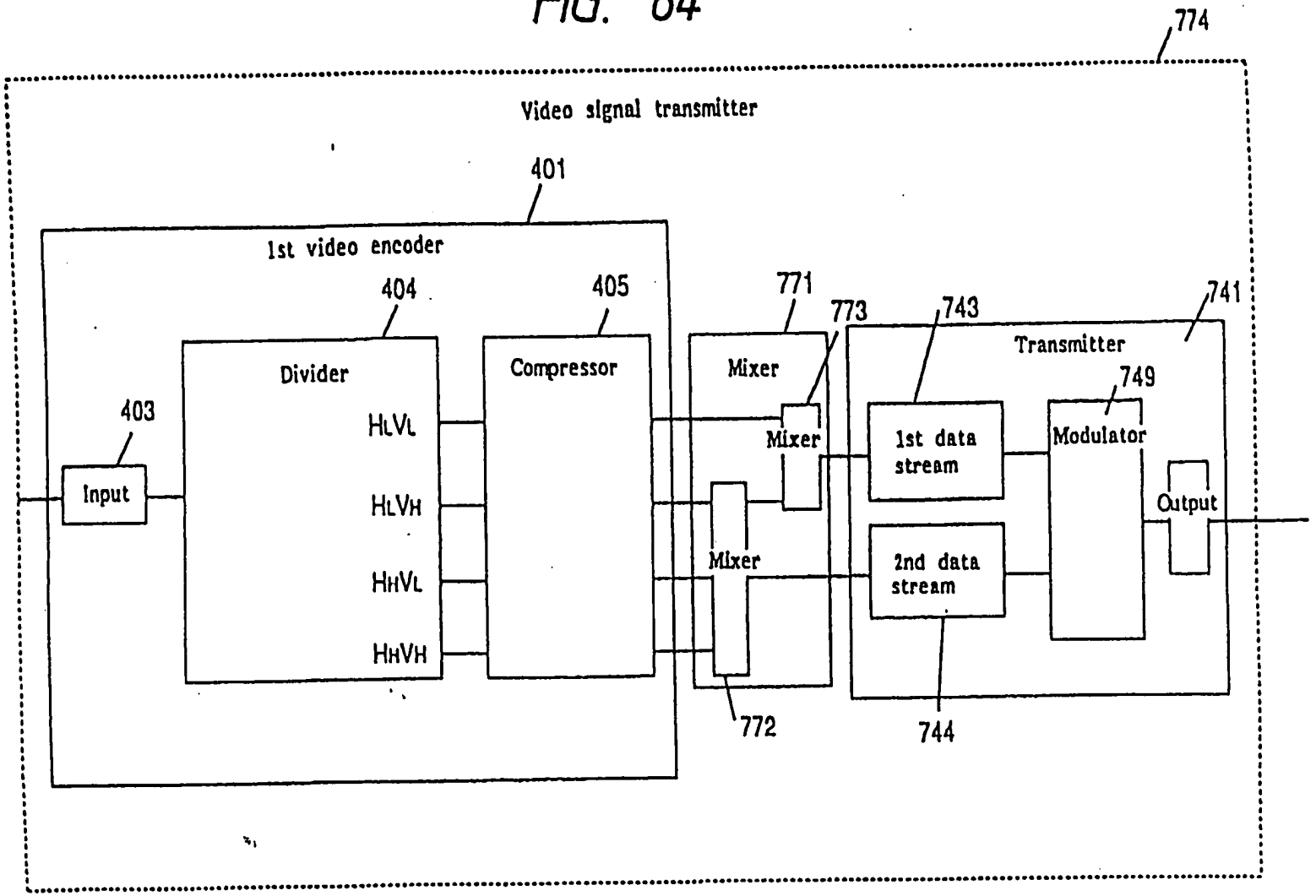

774
Video signal transmitter
401
1st video encoder
404
405
771
773
743
741
Divider
Compressor
Mixer
Transmitter
749
403
HLVL
Mixer
1st data stream
Modulator
Input
HLVH
Output
Mixer
2nd data stream
HHVL
HHVH
772
744

FIG. 65

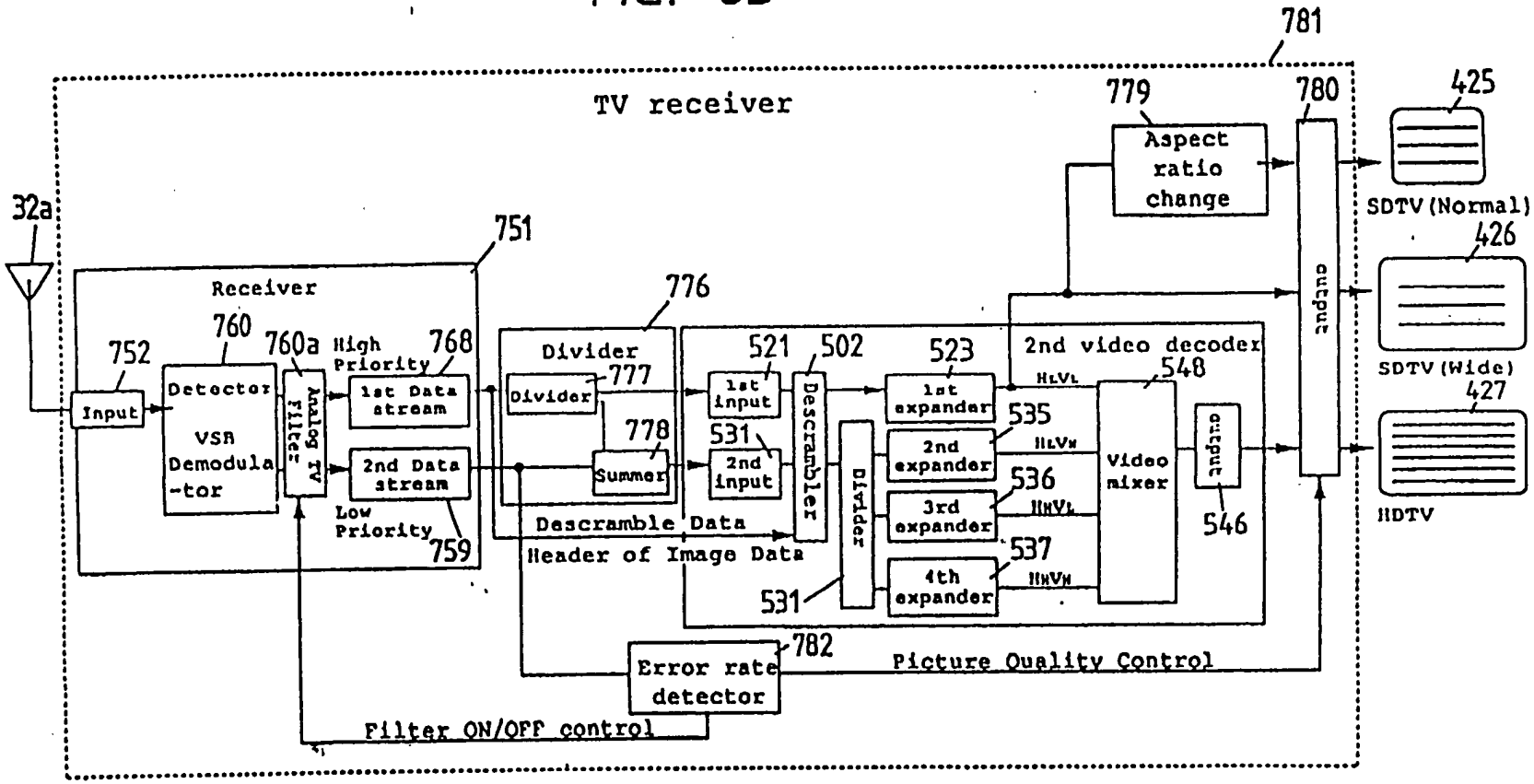

781
TV receiver
779
780
425
Aspect ratio change
output
SDTV (Normal)
426
SDTV (Wide)
427
HDTV
32a
751
Receiver
752
760
760a
High Priority
768
Input
Detector
VSB Demodula-tor
Analog TV Filter
1st Data stream
2nd Data stream
Low Priority
759
776
Divider
777
778
Summer
Descramble Data
Header of Image Data
521
502
523
1st input
2nd input
Descrambler
Divider
531
1st expander
2nd expander
3rd expander
4th expander
2nd video decoder
HLVL
HLVH
HHVL
HHVH
535
536
537
548
Video mixer
output
546
782
Error rate detector
Picture Quality Control
Filter ON/OFF control

FIG. 66

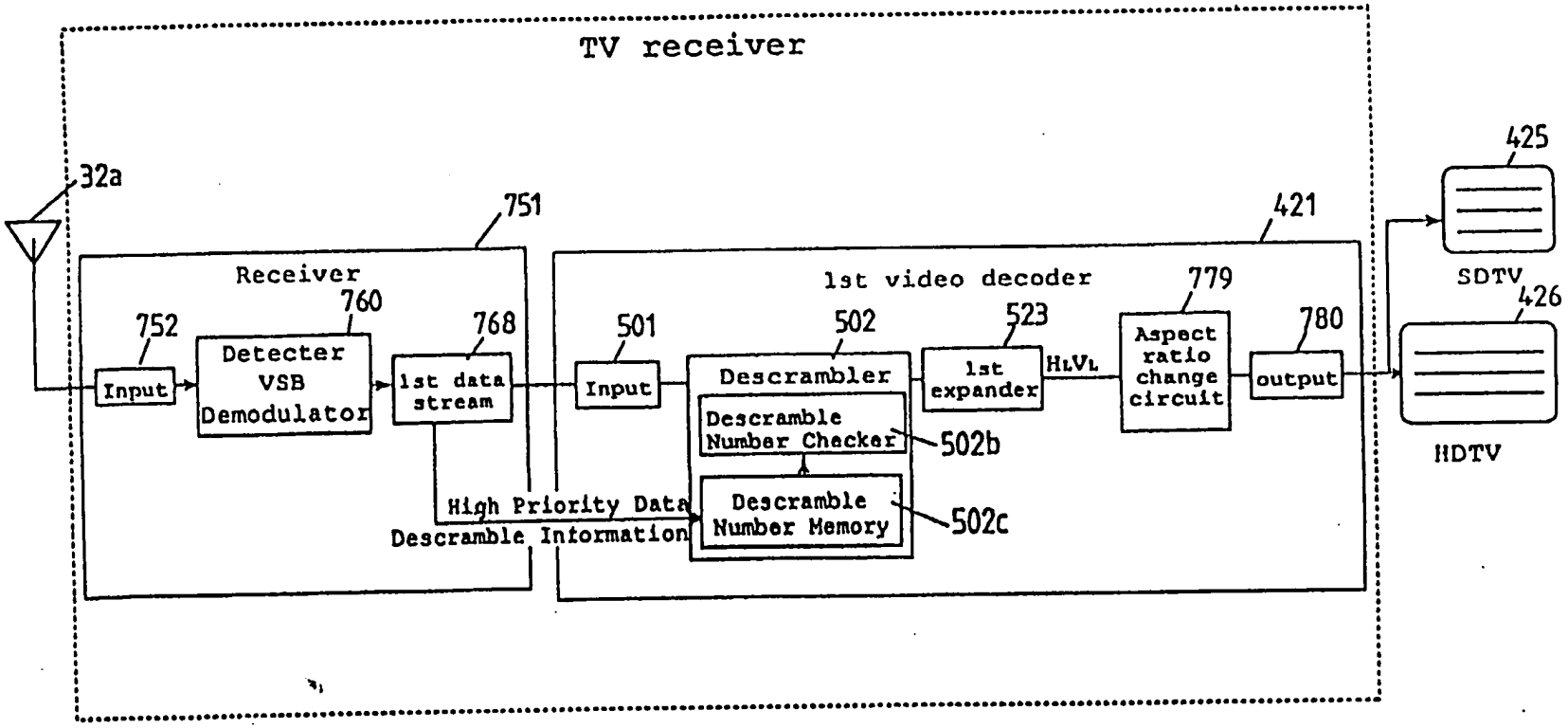

TV receiver
32a
751
Receiver
752
Input
760
Detecter
VSB
Demodulator
768
1st data
stream
High Priority Data
Descramble Information
421
1st video decoder
501
Input
502
Descrambler
Descramble
Number Checker
502b
Descramble
Number Memory
502c
523
1st
expander
HLVL
779
Aspect
ratio
change
circuit
780
output
425
SDTV
426
HDTV

FIG. 67

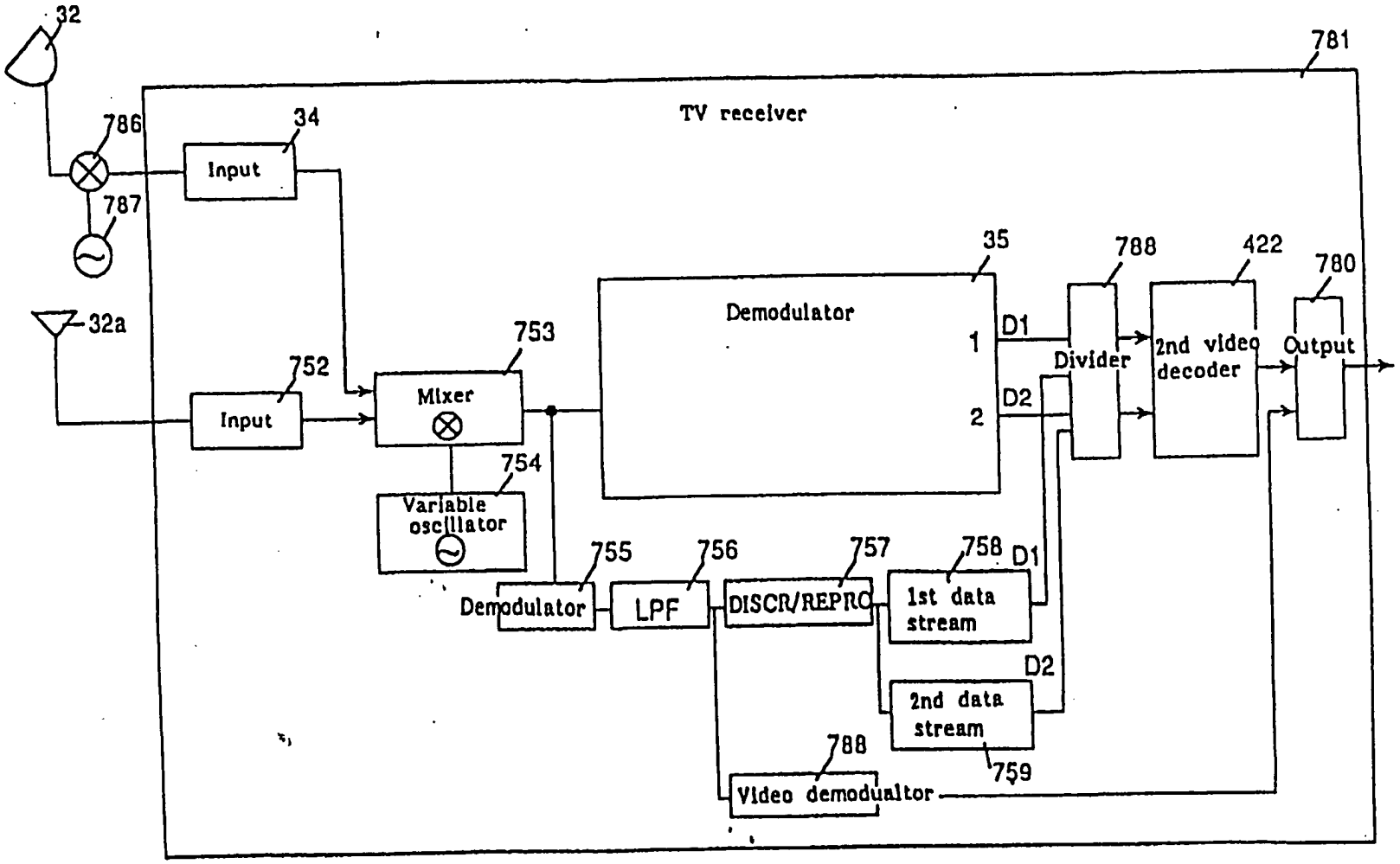

32
781
TV receiver
786
34
Input
787
35
788
422
780
Demodulator
32a
753
D1
1
752
Input
Mixer
Divider
2nd video decoder
Output
2
D2
754
Variable oscillator
755
756
757
758
D1
Demodulator
LPF
DISCR/REPRO
1st data stream
D2
2nd data stream
759
788
Video demodualtor

FIG. 68(a)

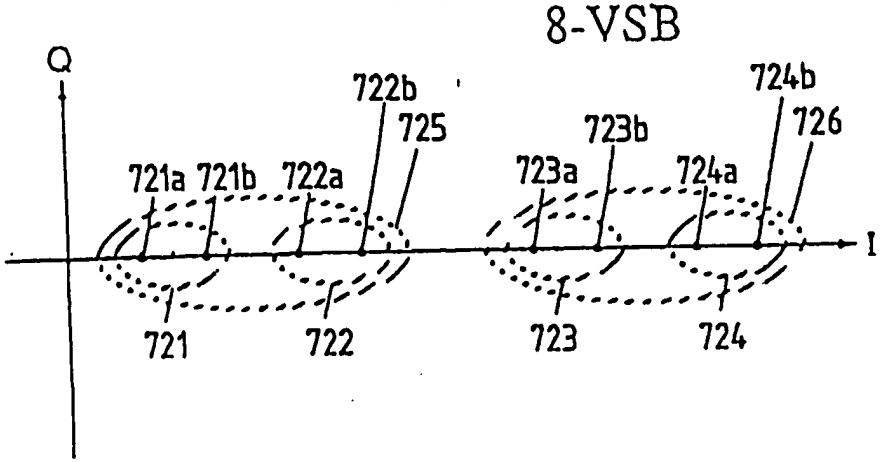


FIG. 68(b)

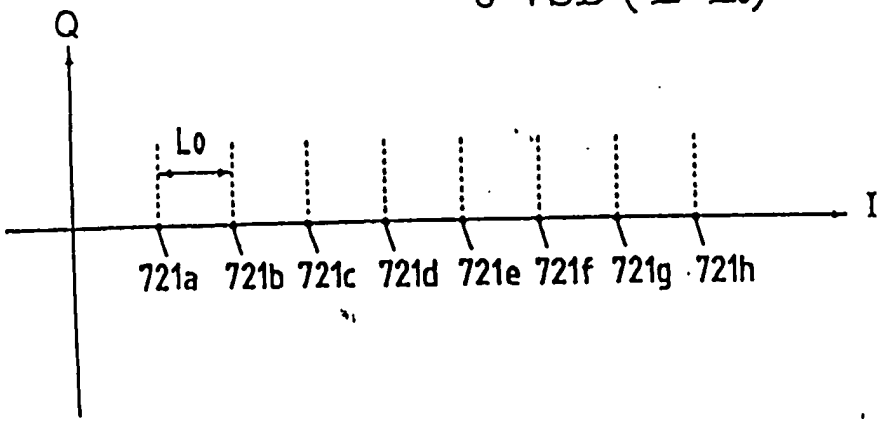


FIG. 68(c)

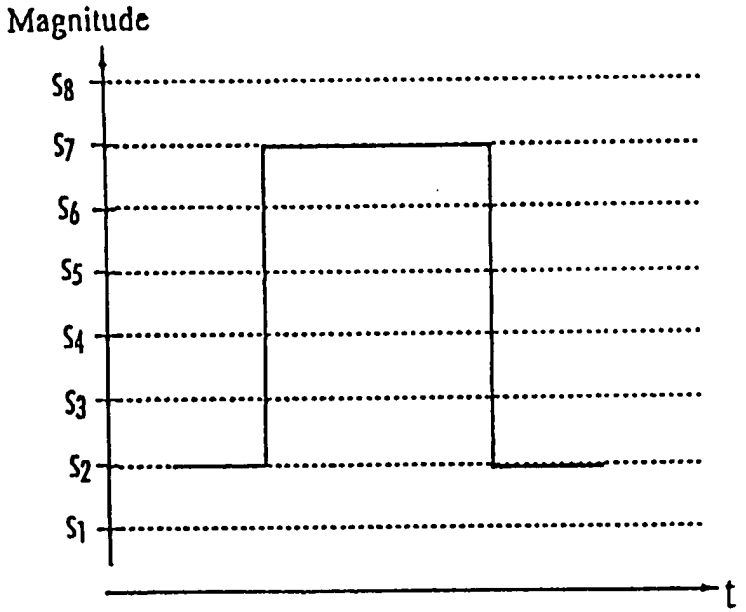


FIG. 69

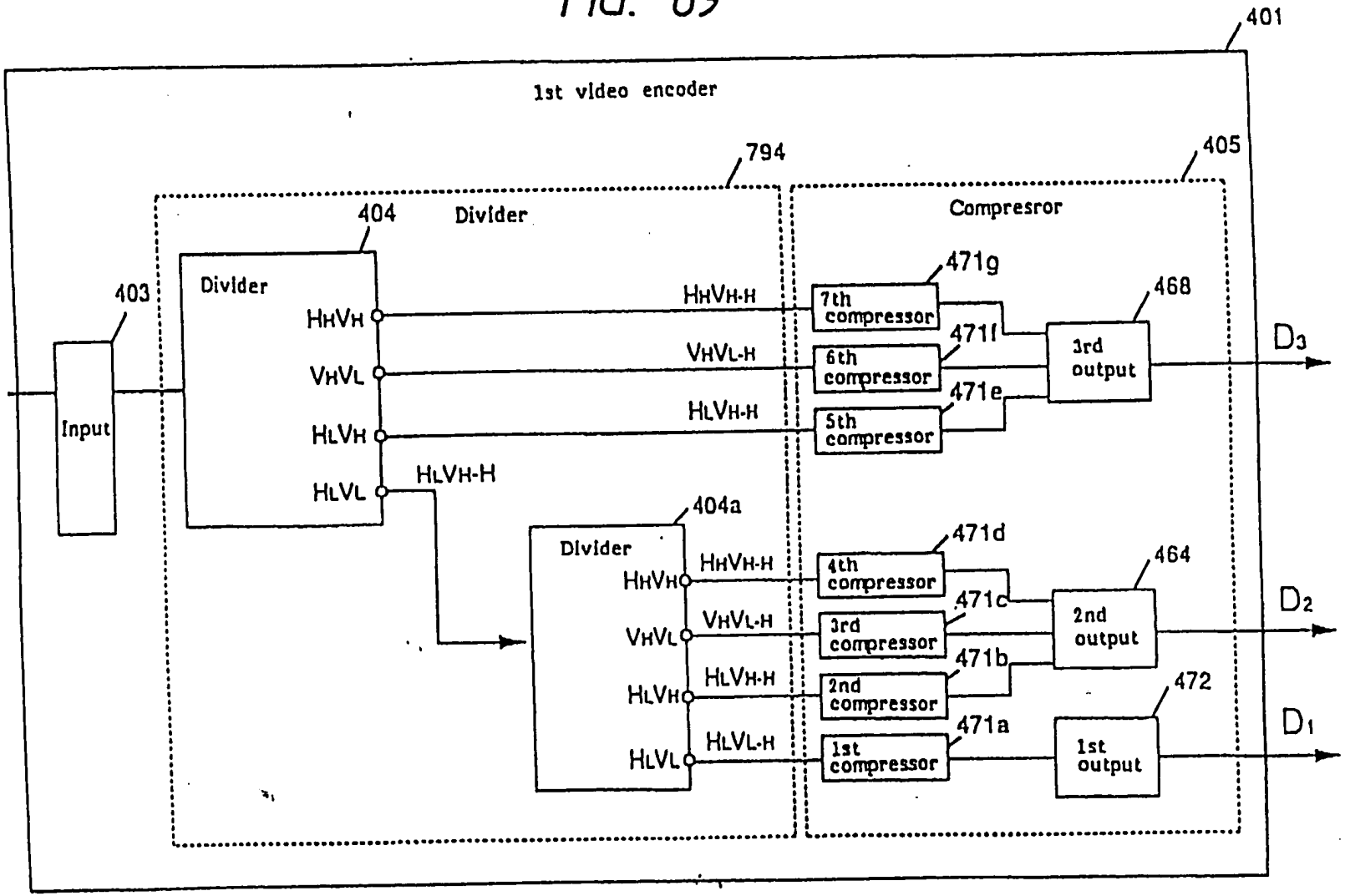

401
1st video encoder
794
405
Divider
Compresror
404
Divider
403
Input
HHVH
VHVL
HLVH
HLVL
HLVH-H
HHVH-H
VHVL-H
HLVH-H
7th compressor
6th compressor
5th compressor
471g
471f
471e
468
3rd output
D3
404a
Divider
HHVH
VHVL
HLVH
HLVL
HHVH-H
VHVL-H
HLVH-H
HLVL-H
4th compressor
3rd compressor
2nd compressor
1st compressor
471d
471c
471b
471a
464
2nd output
D2
472
1st output
D1

FIG. 70

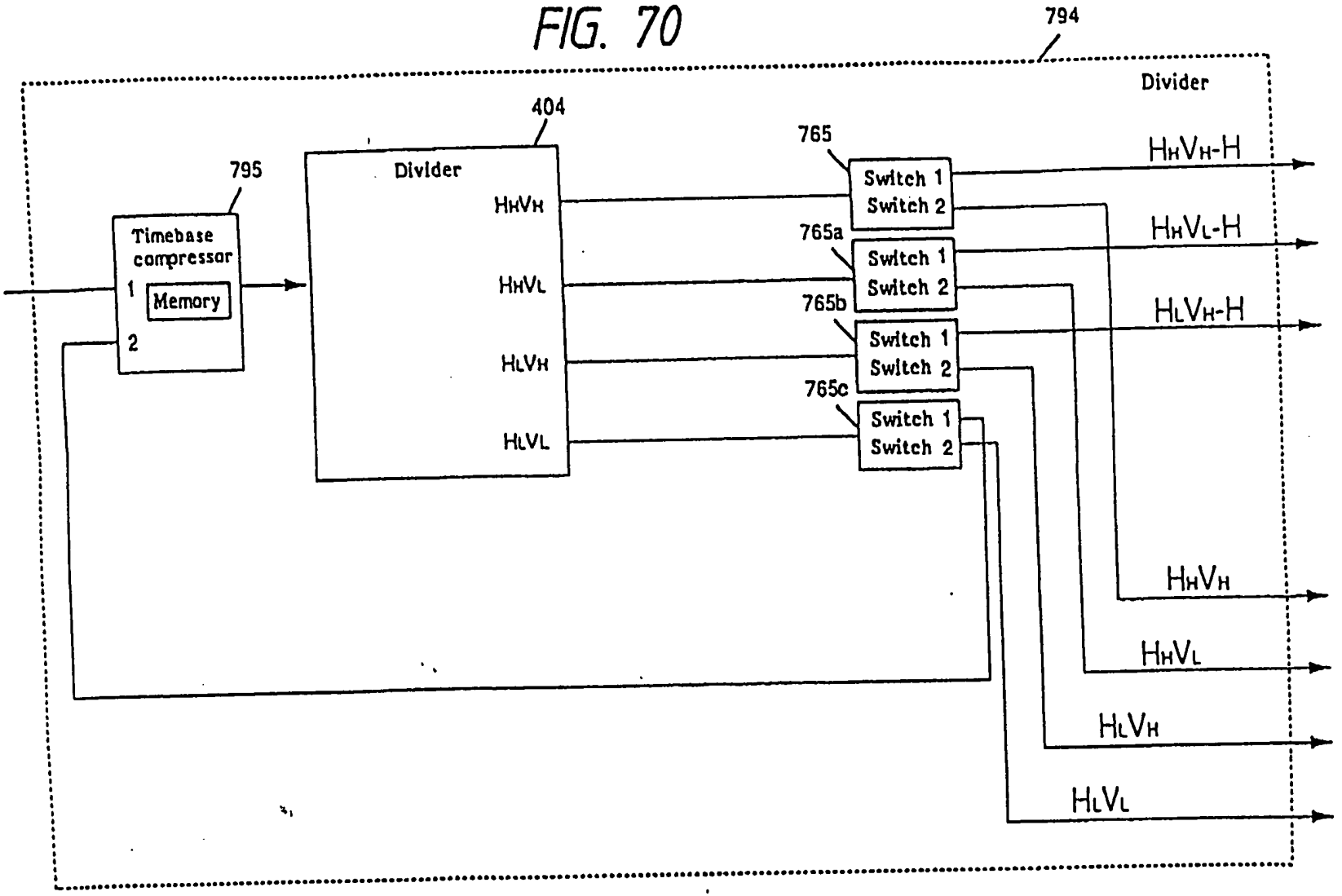

794
Divider
404
Divider
795
Timebase compressor
1
Memory
2
HHVH
HHVL
HLVH
HLVL
765
Switch 1
Switch 2
765a
Switch 1
Switch 2
765b
Switch 1
Switch 2
765c
Switch 1
Switch 2
HHVH-H
HHVL-H
HLVH-H
HHVH
HHVL
HLVH
HLVL

FIG. 71

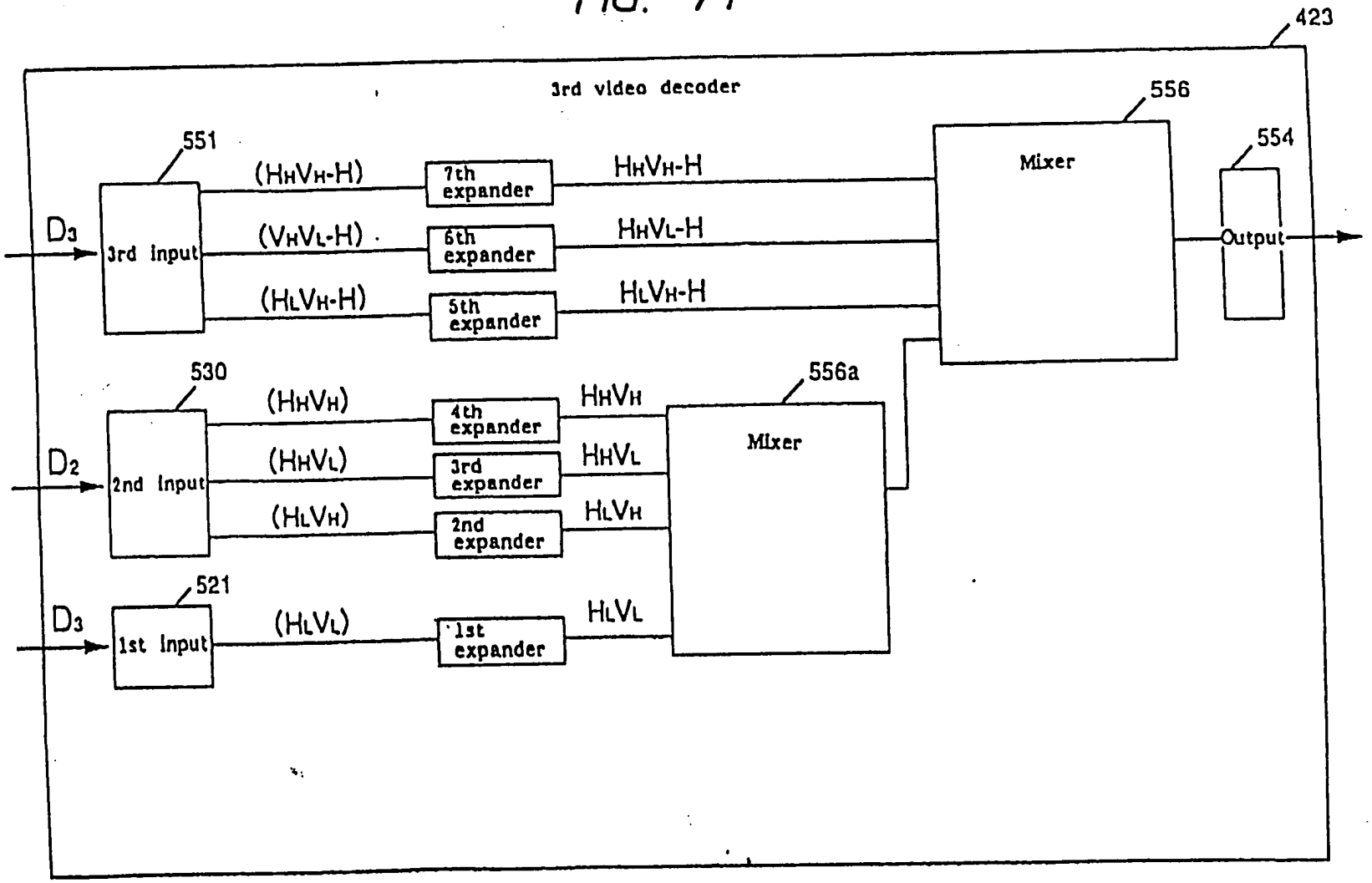

423
3rd video decoder
556
Mixer
554
Output
551
3rd input
D3
(HHVH-H)
7th expander
HHVH-H
(VHVL-H)
6th expander
HHVL-H
(HLVH-H)
5th expander
HLVH-H
530
2nd input
D2
(HHVH)
4th expander
HHVH
(HHVL)
3rd expander
HHVL
(HLVH)
2nd expander
HLVH
556a
Mixer
521
1st input
D3
(HLVL)
1st expander
HLVL

FIG. 72

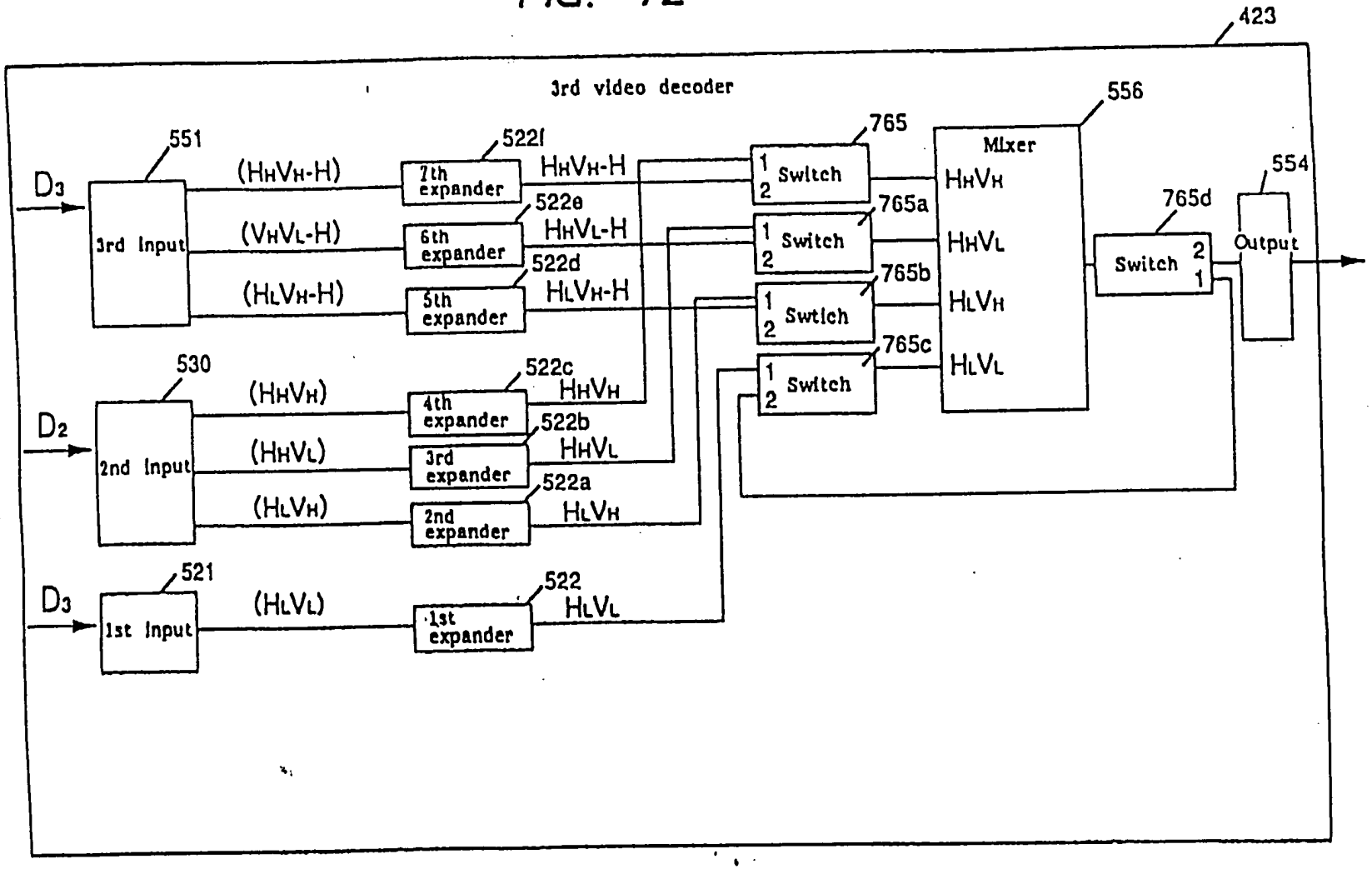

423
3rd video decoder
556
Mixer
765
551
522f
554
765d
765a
765b
765c
530
522c
522b
522a
521
522
D3
D2
D3
3rd Input
2nd Input
1st Input
(HHVH-H)
(VHVL-H)
(HLVH-H)
(HHVH)
(HHVL)
(HLVH)
(HLVL)
7th expander
6th expander
5th expander
4th expander
3rd expander
2nd expander
1st expander
HHVH-H
HHVL-H
HLVH-H
HHVH
HHVL
HLVH
HLVL
1
2
Switch
HHVH
HHVL
HLVH
HLVL
Output

FIG. 73

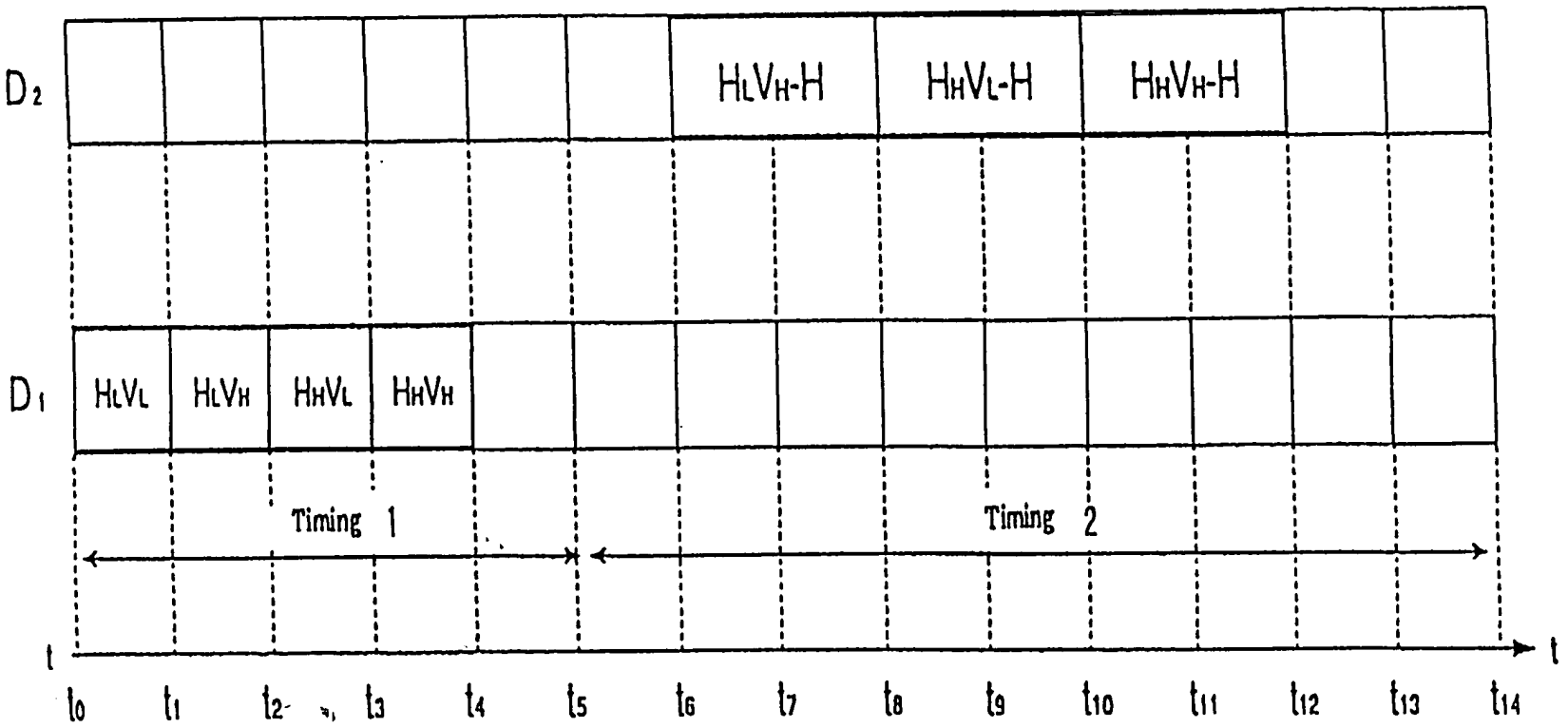

D2
D1
HLVH-H
HHVL-H
HHVH-H
HLVL
HLVH
HHVL
HHVH
Timing 1
Timing 2
t
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14

FIG. 74(a)

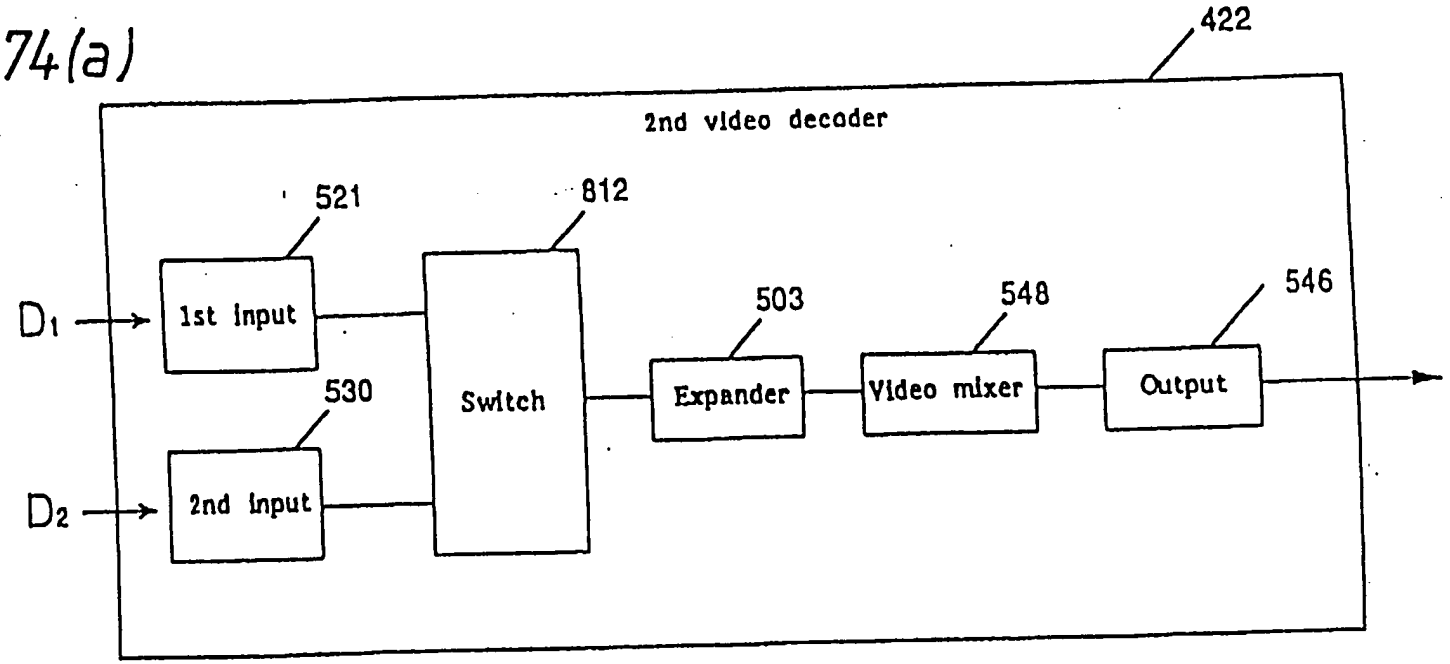


FIG. 74(b)

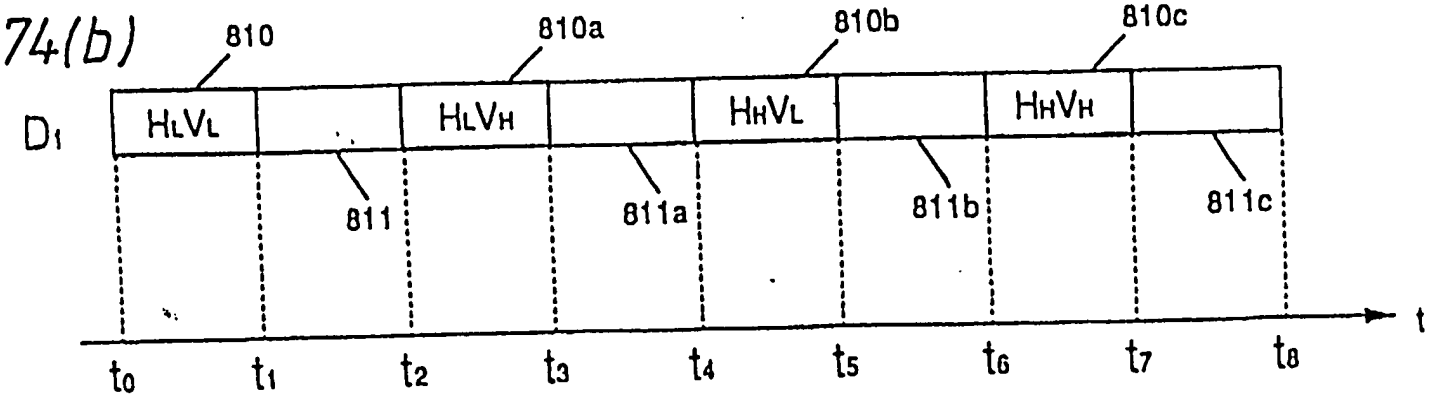


FIG. 75

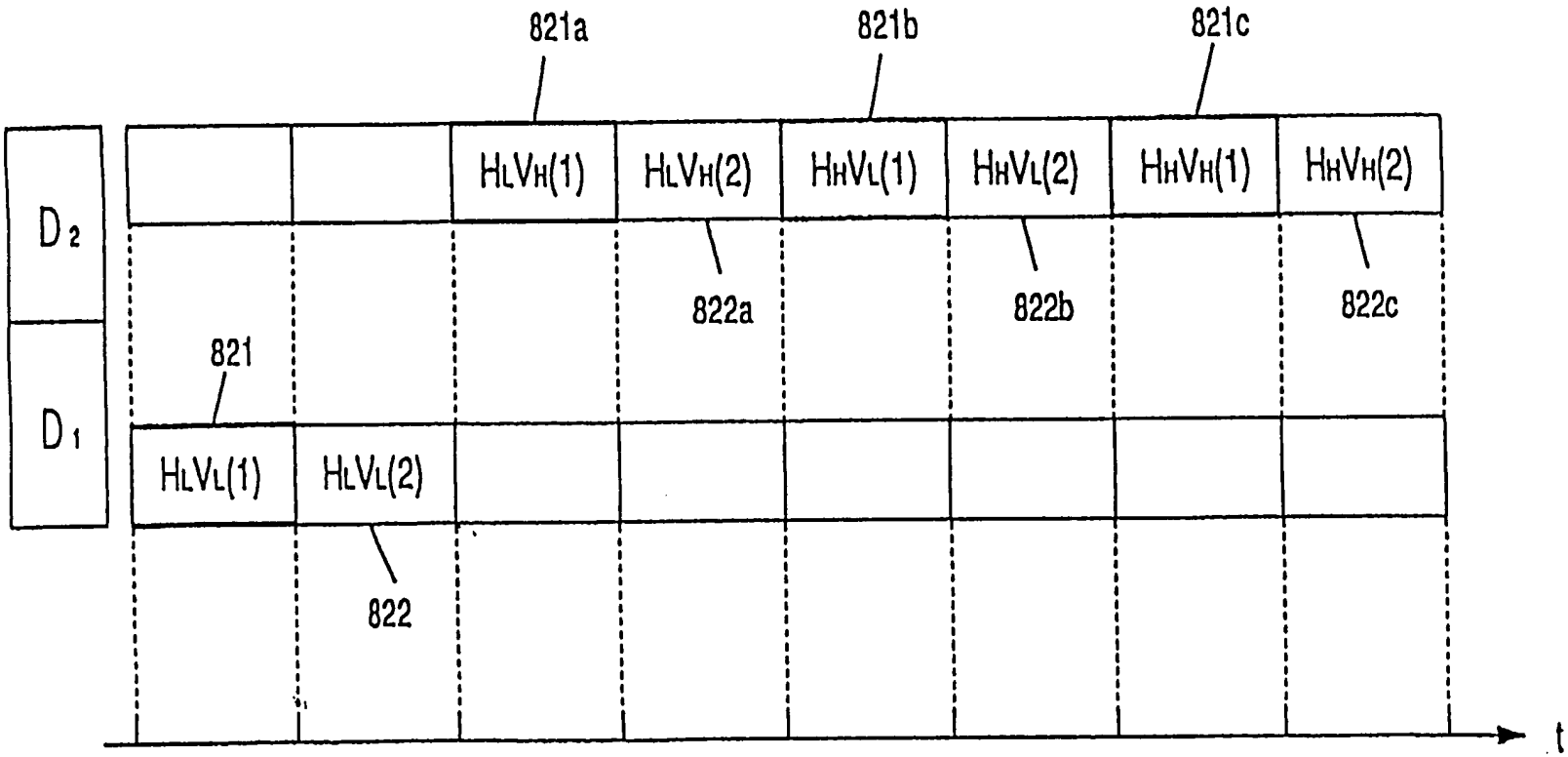

821a
821b
821c
D2
D1
HLVH(1)
HLVH(2)
HHVL(1)
HHVL(2)
HHVH(1)
HHVH(2)
822a
822b
822c
821
HLVL(1)
HLVL(2)
822
t

FIG. 76

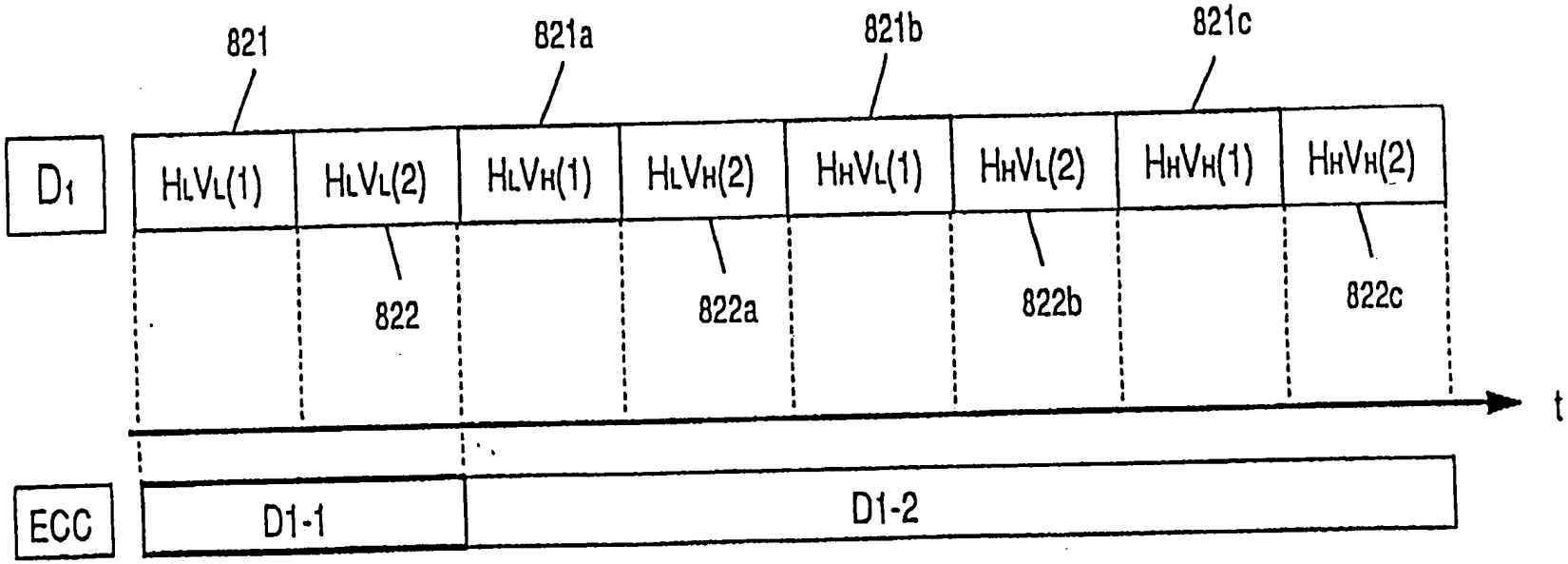

821
821a
821b
821c
D1
HLVL(1)
HLVL(2)
HLVH(1)
HLVH(2)
HHVL(1)
HHVL(2)
HHVH(1)
HHVH(2)
822
822a
822b
822c
t
ECC
D1-1
D1-2

FIG. 77

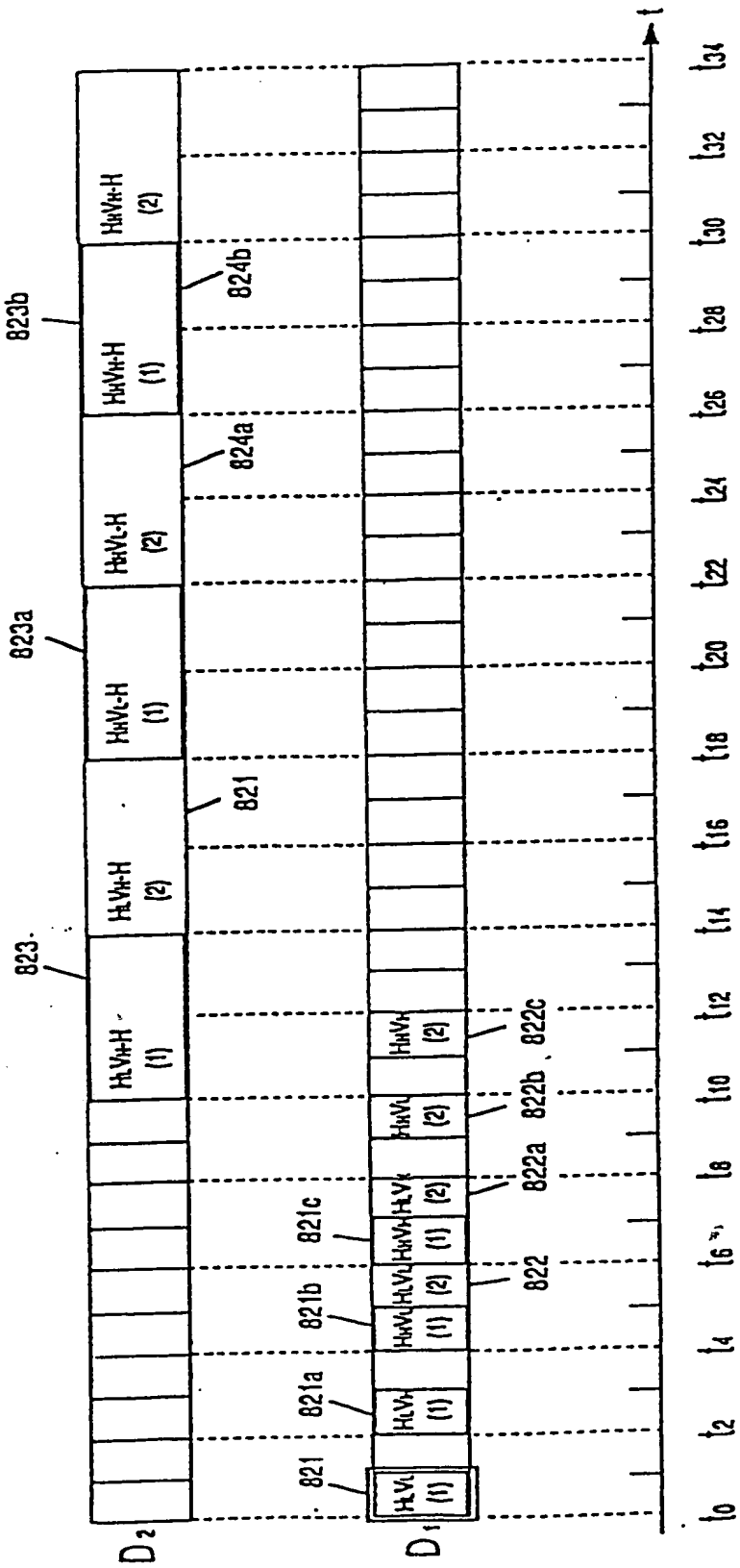

D2
D1
t
t0
t2
t4
t6
t8
t10
t12
t14
t16
t18
t20
t22
t24
t26
t28
t30
t32
t34
823
823a
823b
821
821a
821b
821c
822
822a
822b
822c
824a
824b
HLVL (1)
HLVH (1)
HHVL (1)
HLVL (2)
HHVH (1)
HLVH (2)
HHVL (2)
HHVH (2)

FIG. 78

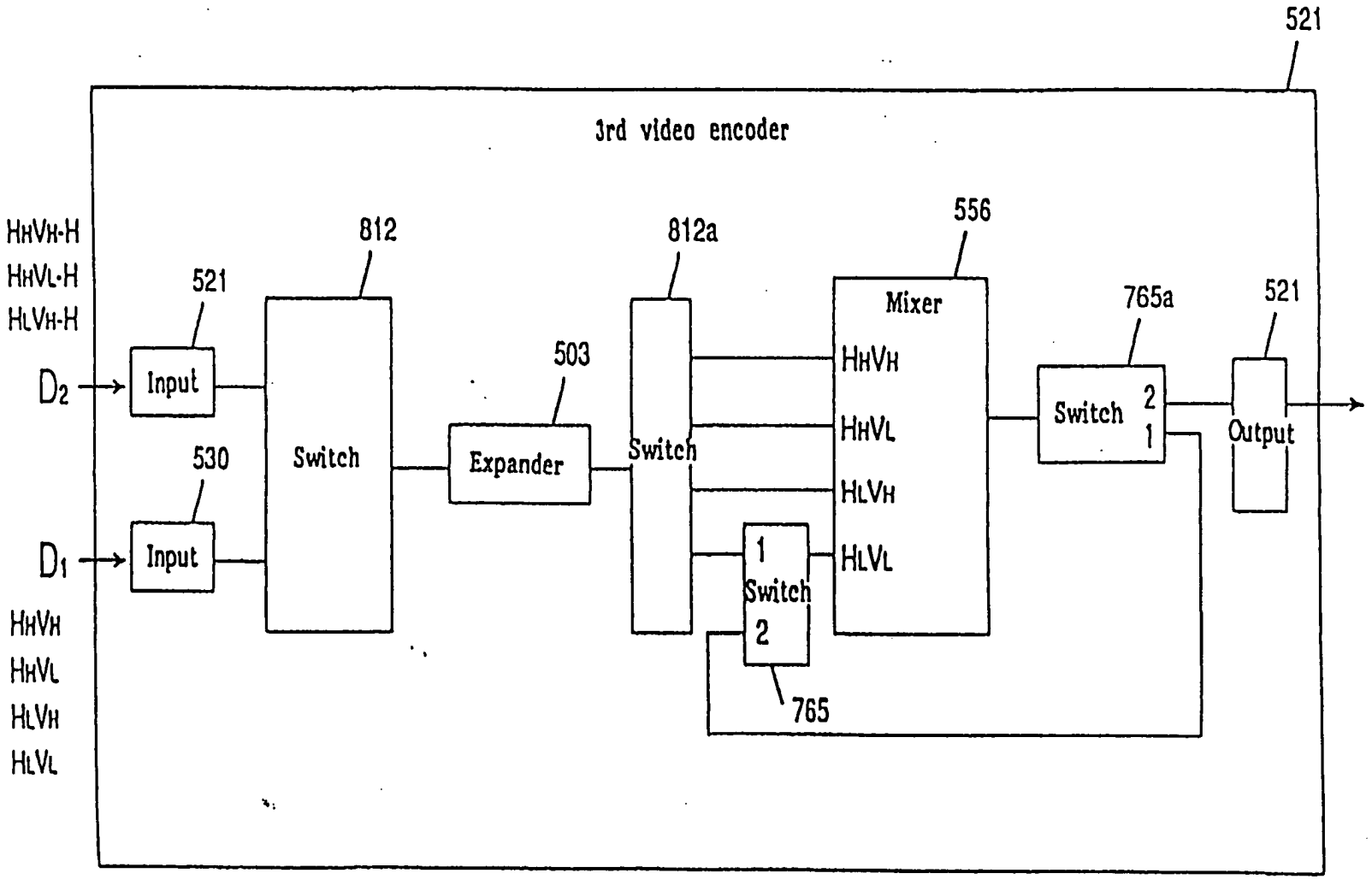

521
3rd video encoder
HHVH-H
HHVL-H
HLVH-H
D2
521
Input
812
Switch
503
Expander
812a
Switch
556
Mixer
HHVH
HHVL
HLVH
HLVL
765a
Switch
2
1
521
Output
D1
530
Input
HHVH
HHVL
HLVH
HLVL
1
Switch
2
765

FIG. 79

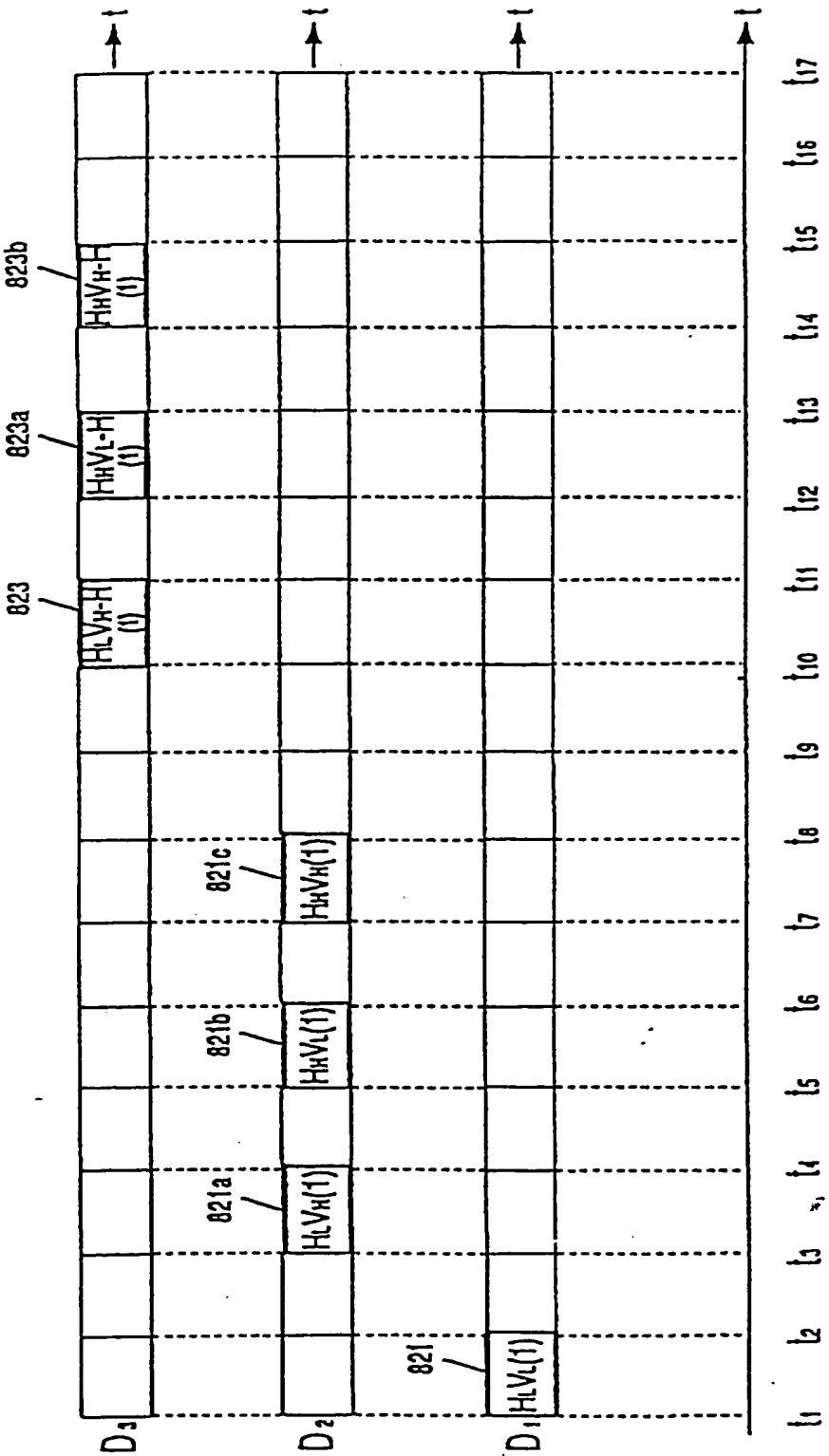

t
t
t
t
823b
HHVH-H (1)
823a
HHVL-H (1)
823
HLVH-H (1)
821c
HHVH(1)
821b
HHVL(1)
821a
HLVH(1)
821
HLVL(1)
D3
D2
D1
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14
t15
t16
t17

FIG. 80

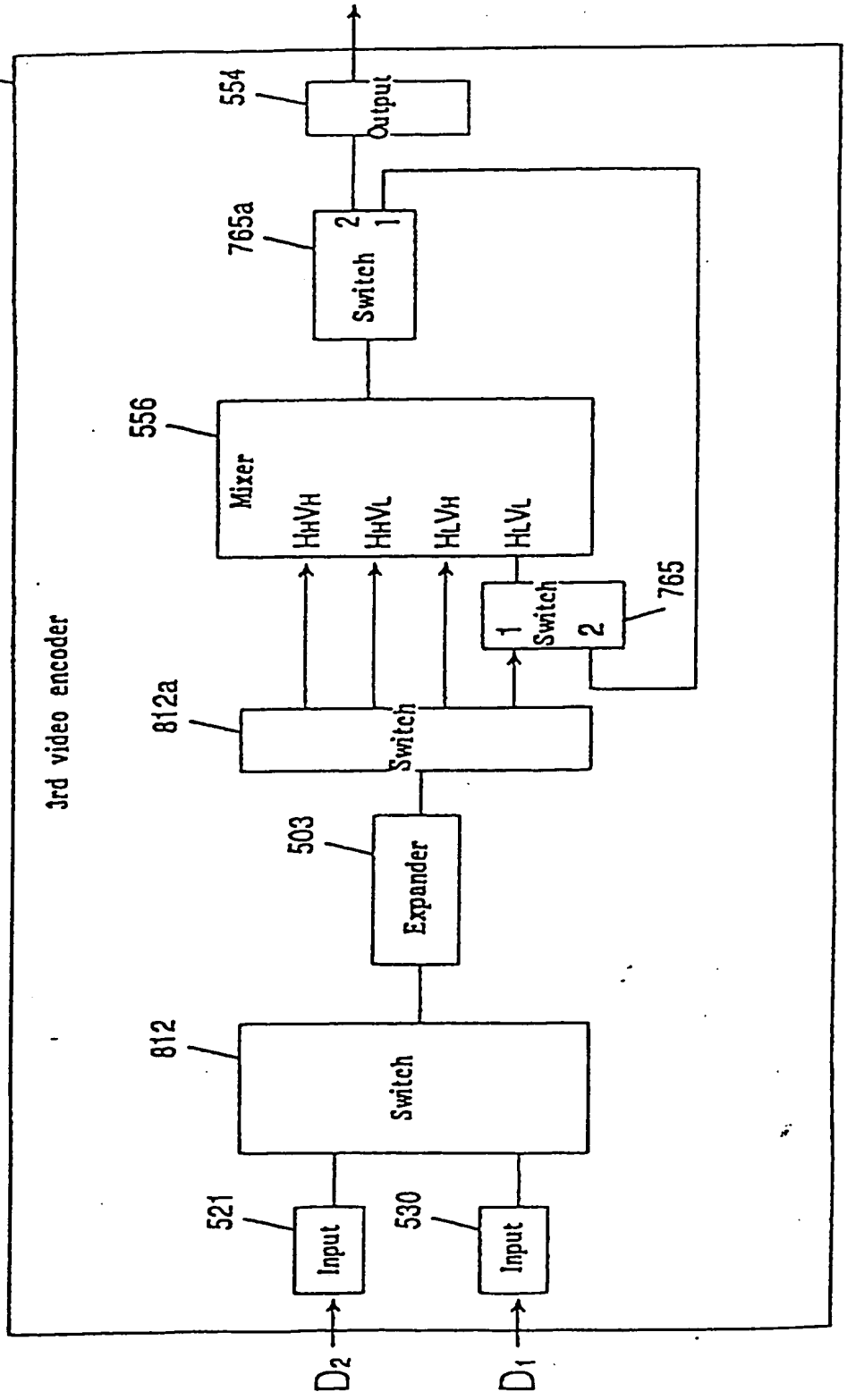

423
3rd video encoder
554
Output
765a
Switch
2
1
556
Mixer
HHVH
HHVL
HLVH
HLVL
765
Switch
1
2
812a
Switch
503
Expander
812
Switch
521
Input
530
Input
D2
D1

FIG. 81

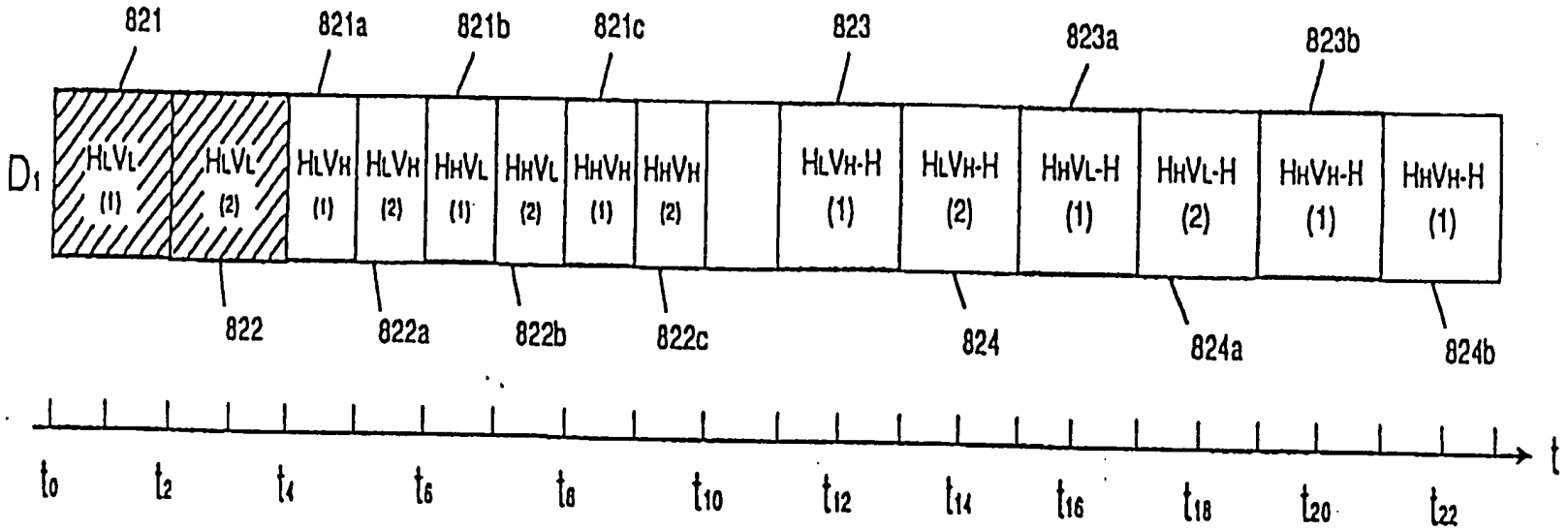

821
821a
821b
821c
823
823a
823b
D1
HLVL (1)
HLVL (2)
HLVH (1)
HLVH (2)
HHVL (1)
HHVL (2)
HHVH (1)
HHVH (2)
HLVH-H (1)
HLVH-H (2)
HHVL-H (1)
HHVL-H (2)
HHVH-H (1)
HHVH-H (1)
822
822a
822b
822c
824
824a
824b
t
t0
t2
t4
t6
t8
t10
t12
t14
t16
t18
t20
t22

FIG. 82

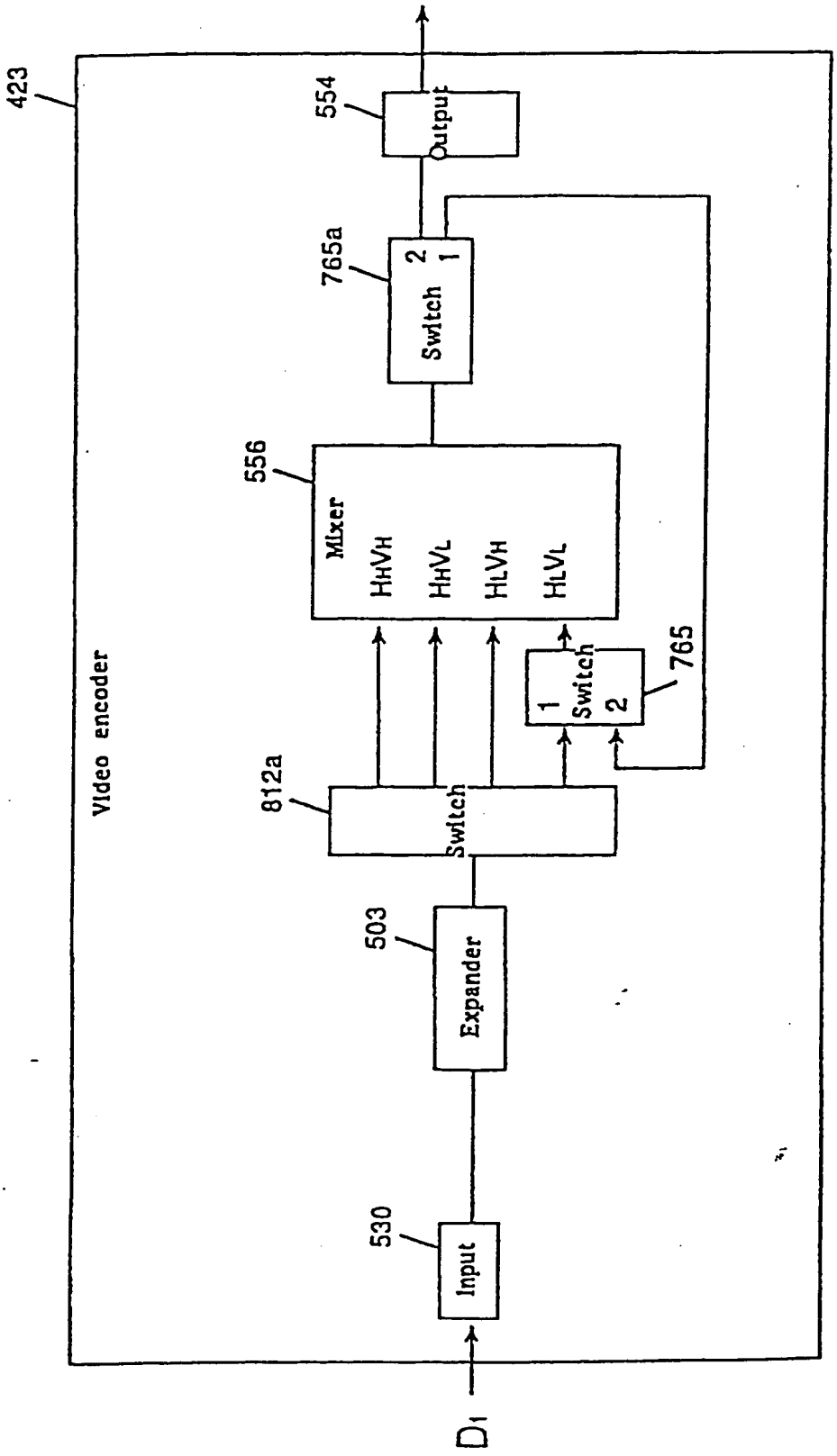

423
Video encoder
554
Output
765a
Switch
2
1
556
Mixer
HHVH
HHVL
HLVH
HLVL
765
Switch
1
2
812a
Switch
503
Expander
530
Input
D1

FIG. 83

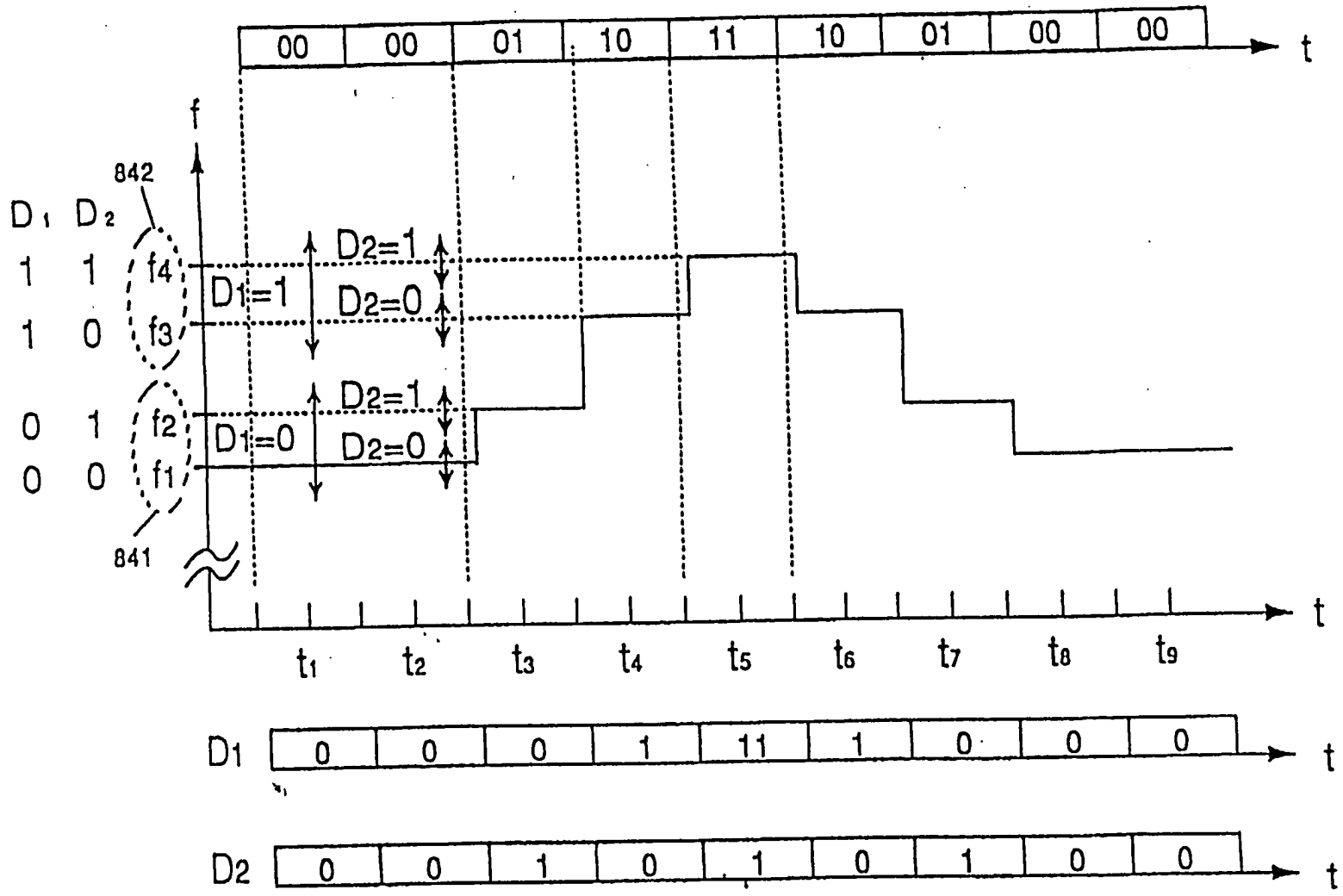

00
00
01
10
11
10
01
00
00
t
f
842
D1 D2
1 1
1 0
0 1
0 0
f4
f3
f2
f1
841
D1=1
D1=0
D2=1
D2=0
D2=1
D2=0
t
t1
t2
t3
t4
t5
t6
t7
t8
t9
D1
0
0
0
1
11
1
0
0
0
t
D2
0
0
1
0
1
0
1
0
0
t

FIG. 84

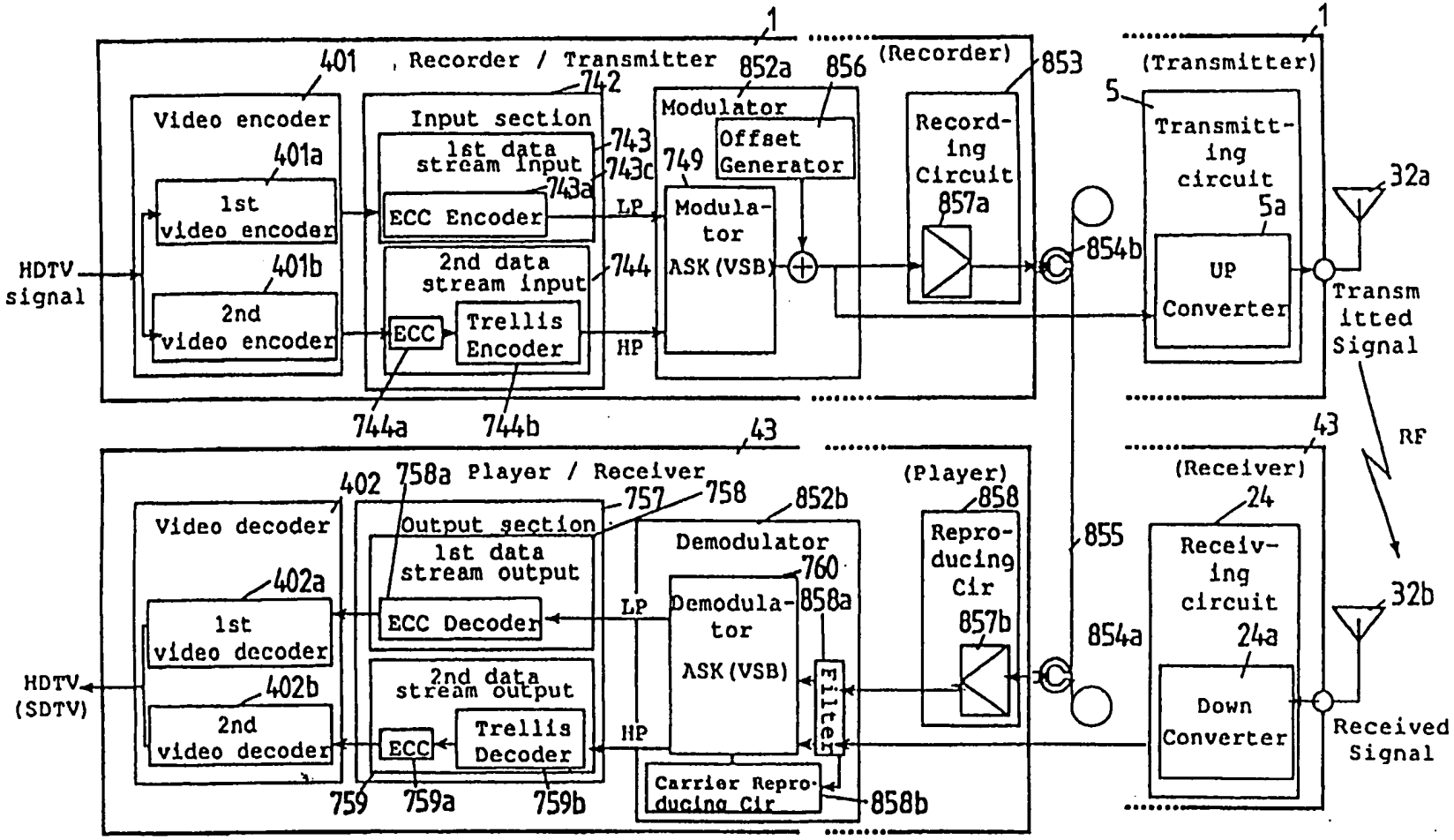
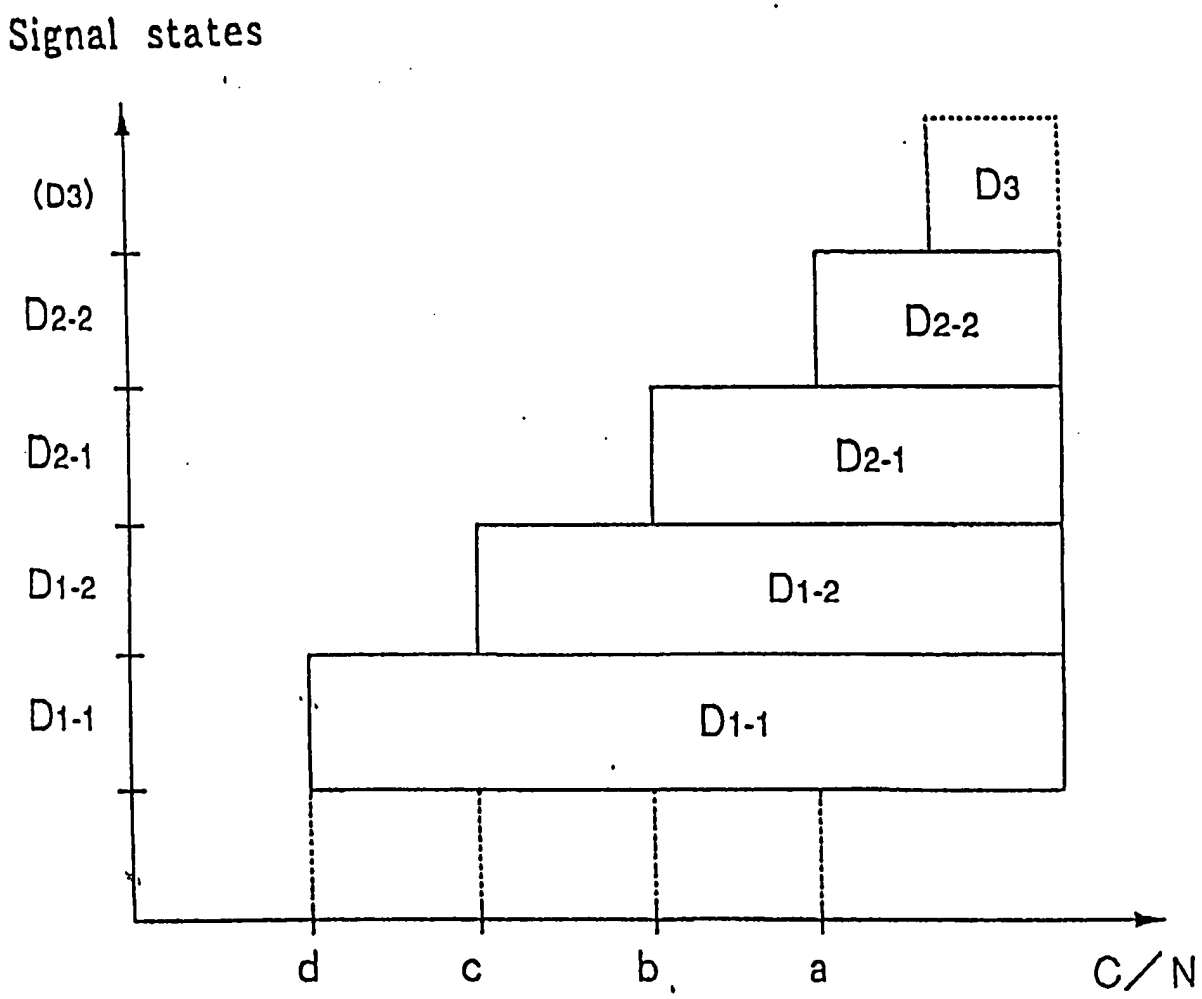

1
Recorder / Transmitter
(Recorder)
(Transmitter)
401
Video encoder
401a
1st video encoder
401b
2nd video encoder
HDTV signal
742
Input section
1st data stream input
743
743c
743a
ECC Encoder
2nd data stream input
744
ECC
Trellis Encoder
744a
744b
LP
HP
852a
856
Modulator
Offset Generator
749
Modulator ASK (VSB)
853
Recording Circuit
857a
854b
5
Transmitting circuit
5a
UP Converter
32a
Transmitted Signal
RF
43
Player / Receiver
(Player)
(Receiver)
402
Video decoder
402a
1st video decoder
402b
2nd video decoder
HDTV (SDTV)
758a
757
758
Output section
1st data stream output
2nd data stream output
ECC Decoder
Trellis Decoder
759
759a
759b
852b
Demodulator
760
Demodulator ASK (VSB)
858a
Filter
Carrier Reproducing Cir
858b
858
Reproducing Cir
857b
855
854a
24
Receiving circuit
24a
Down Converter
32b
Received Signal

FIG. 85



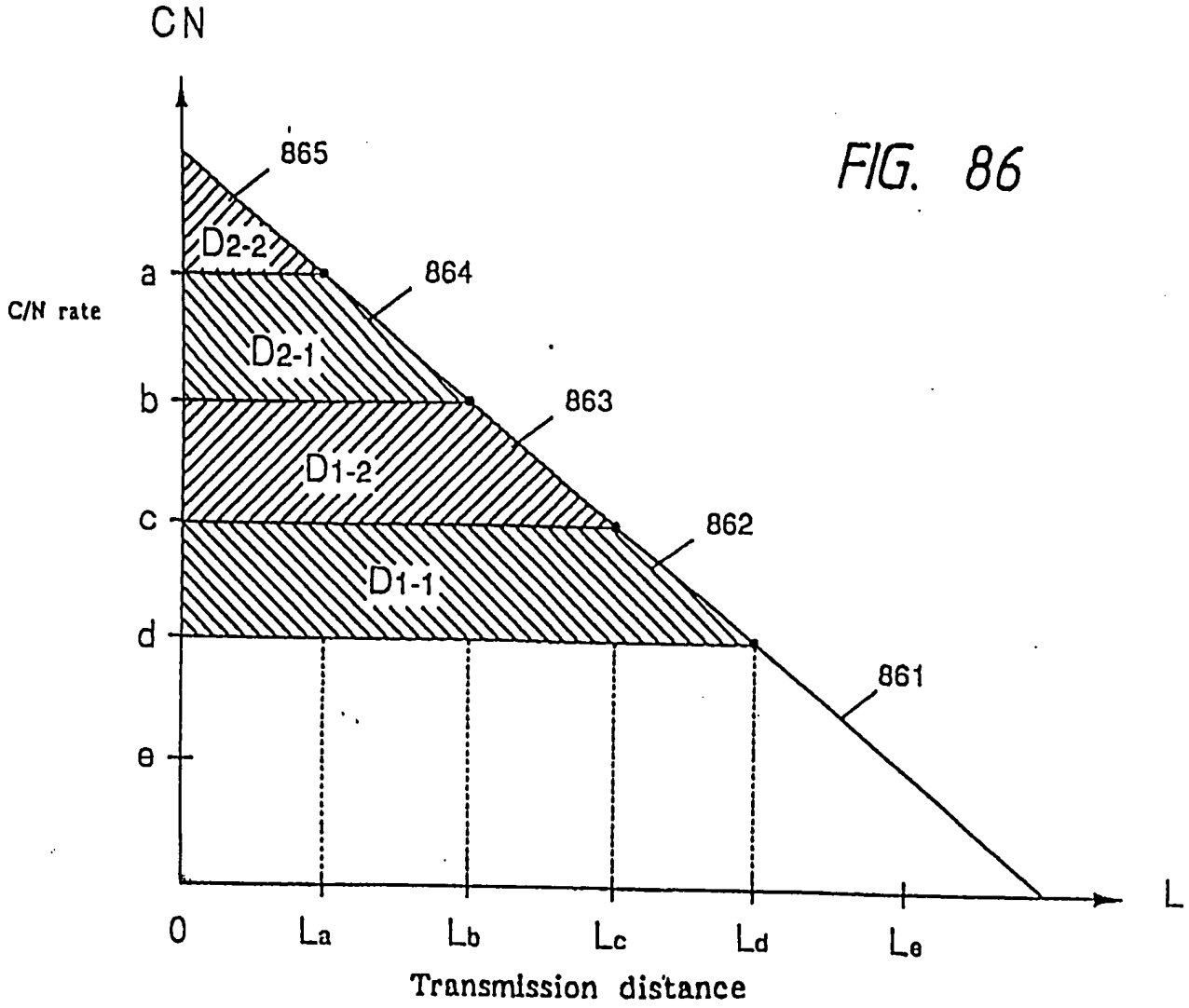

CN
865
D2-2
a
C/N rate
864
D2-1
b
863
D1-2
c
862
D1-1
d
861
e
L
0
La
Lb
Lc
Ld
Le
Transmission distance

FIG. 86

FIG. 87

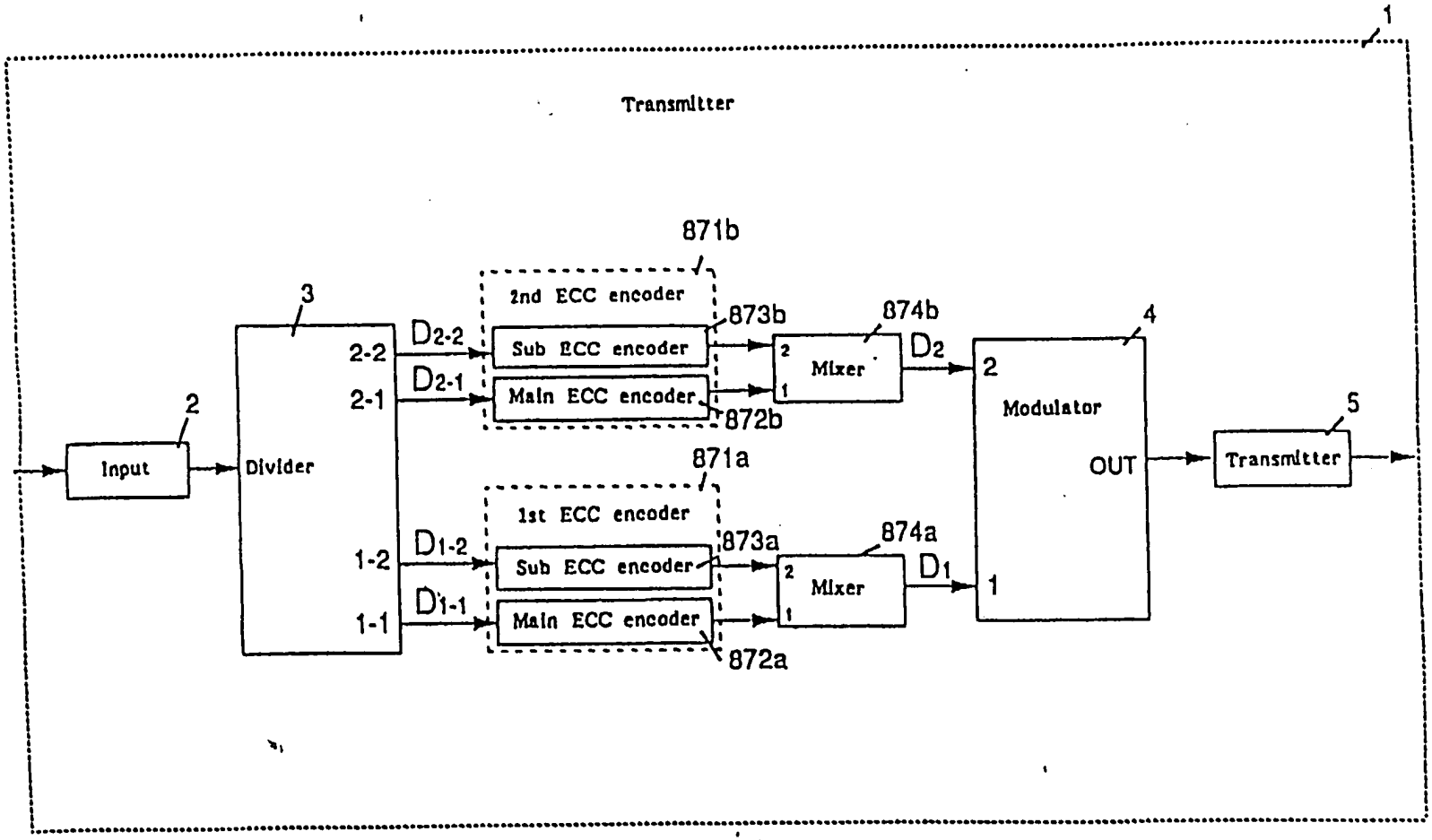

1
Transmitter
871b
2nd ECC encoder
873b
874b
3
2-2
D2-2
Sub ECC encoder
2
Mixer
D2
4
2-1
D2-1
Main ECC encoder
1
2
Modulator
2
872b
Input
Divider
OUT
5
Transmitter
871a
1st ECC encoder
873a
874a
1-2
D1-2
Sub ECC encoder
2
Mixer
D1
1
1-1
D1-1
Main ECC encoder
1
872a

FIG. 88

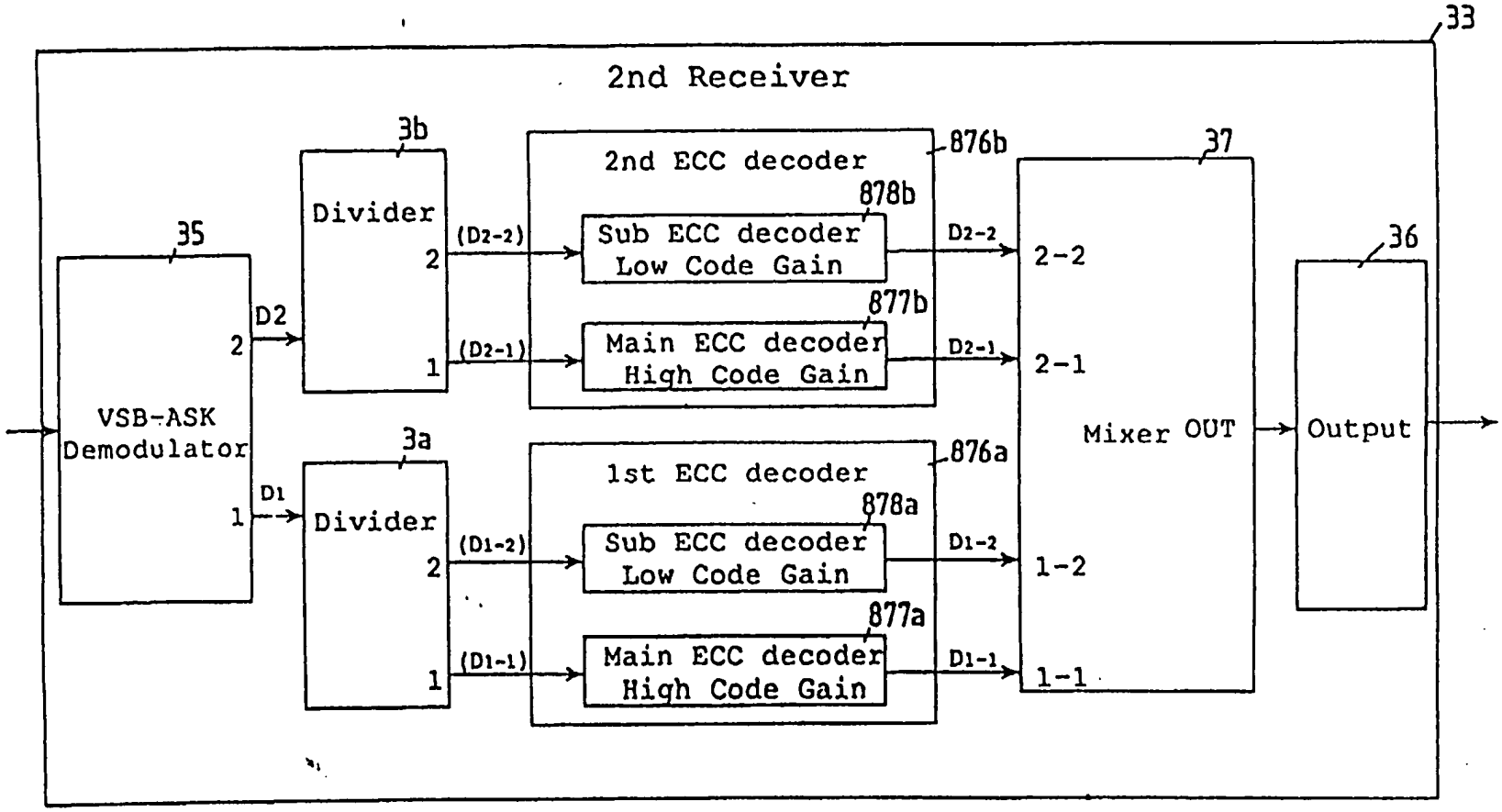
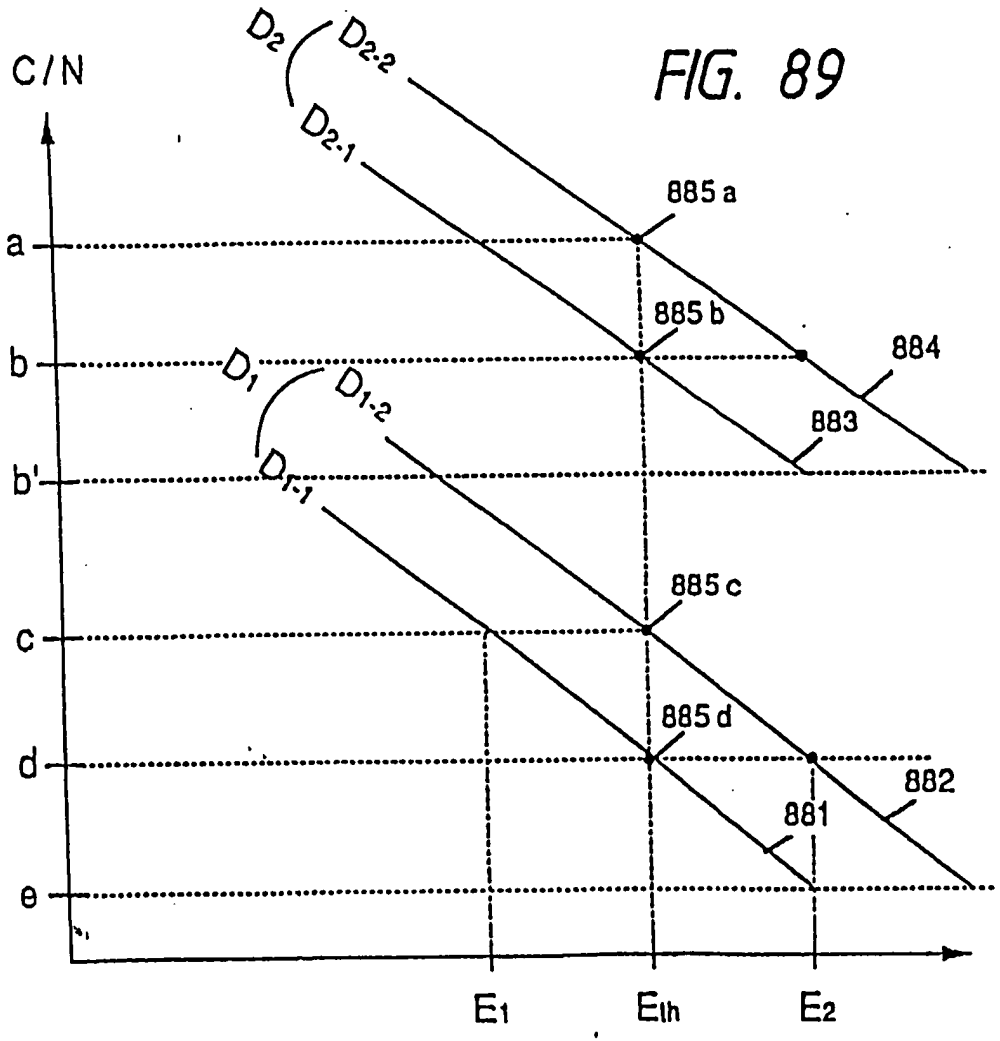

33
2nd Receiver
35
VSB-ASK Demodulator
2
1
D2
D1
3b
Divider
2
1
3a
Divider
2
1
(D2-2)
(D2-1)
(D1-2)
(D1-1)
876b
2nd ECC decoder
878b
Sub ECC decoder Low Code Gain
877b
Main ECC decoder High Code Gain
876a
1st ECC decoder
878a
Sub ECC decoder Low Code Gain
877a
Main ECC decoder High Code Gain
D2-2
D2-1
D1-2
D1-1
37
2-2
2-1
Mixer OUT
1-2
1-1
36
Output

FIG. 89



Error rate after error correction

FIG. 90

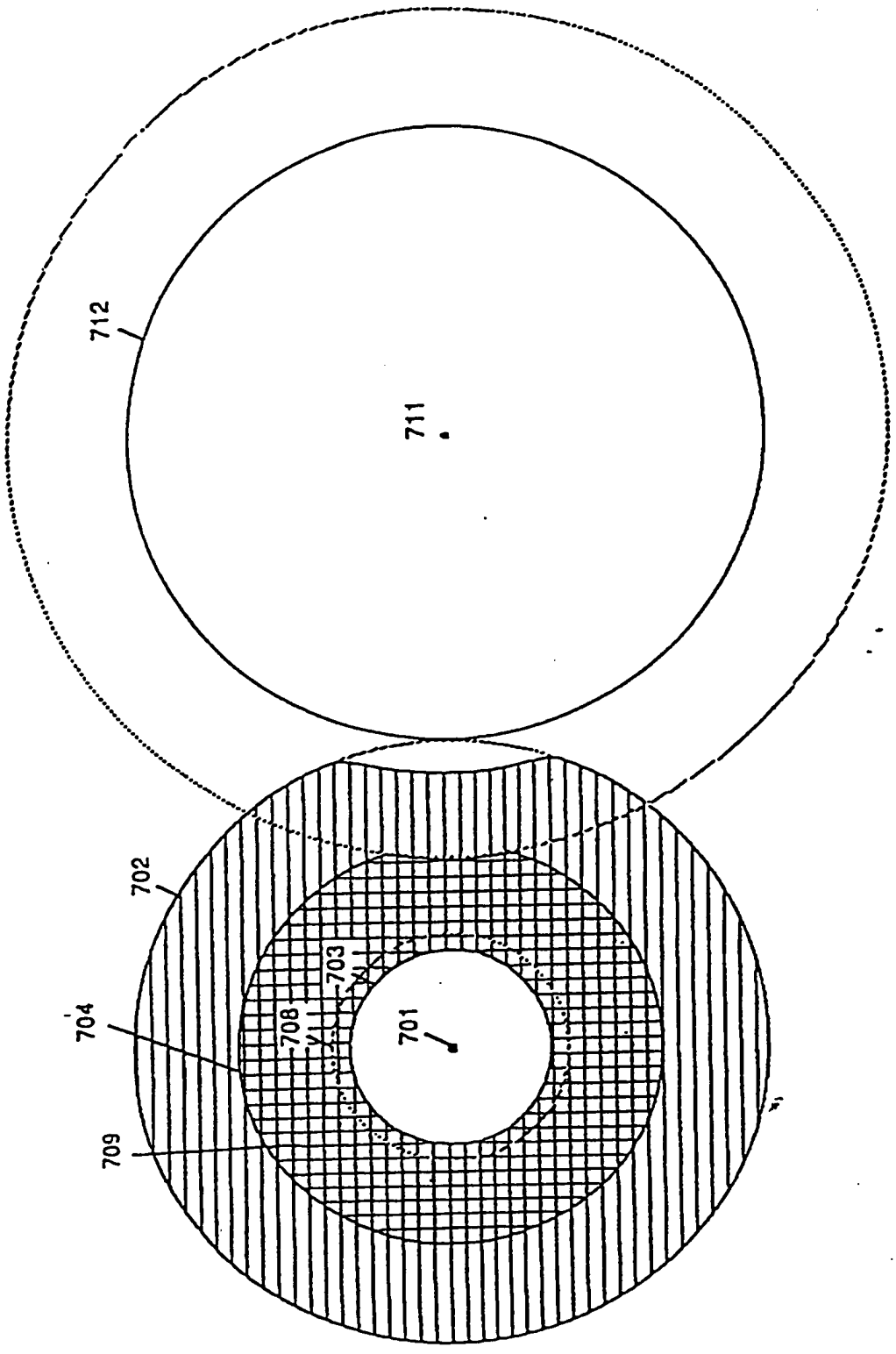


FIG. 91

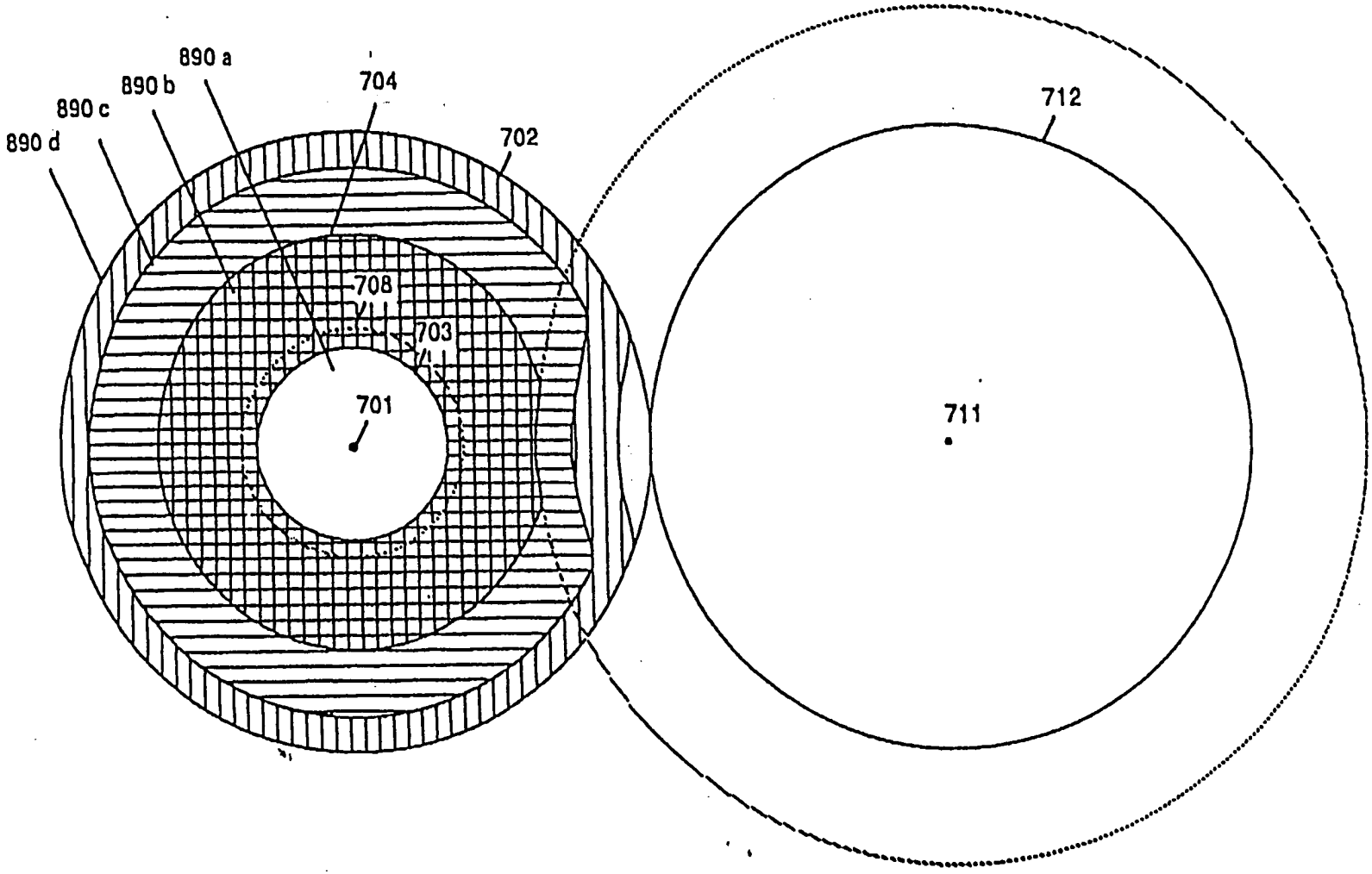


FIG. 92

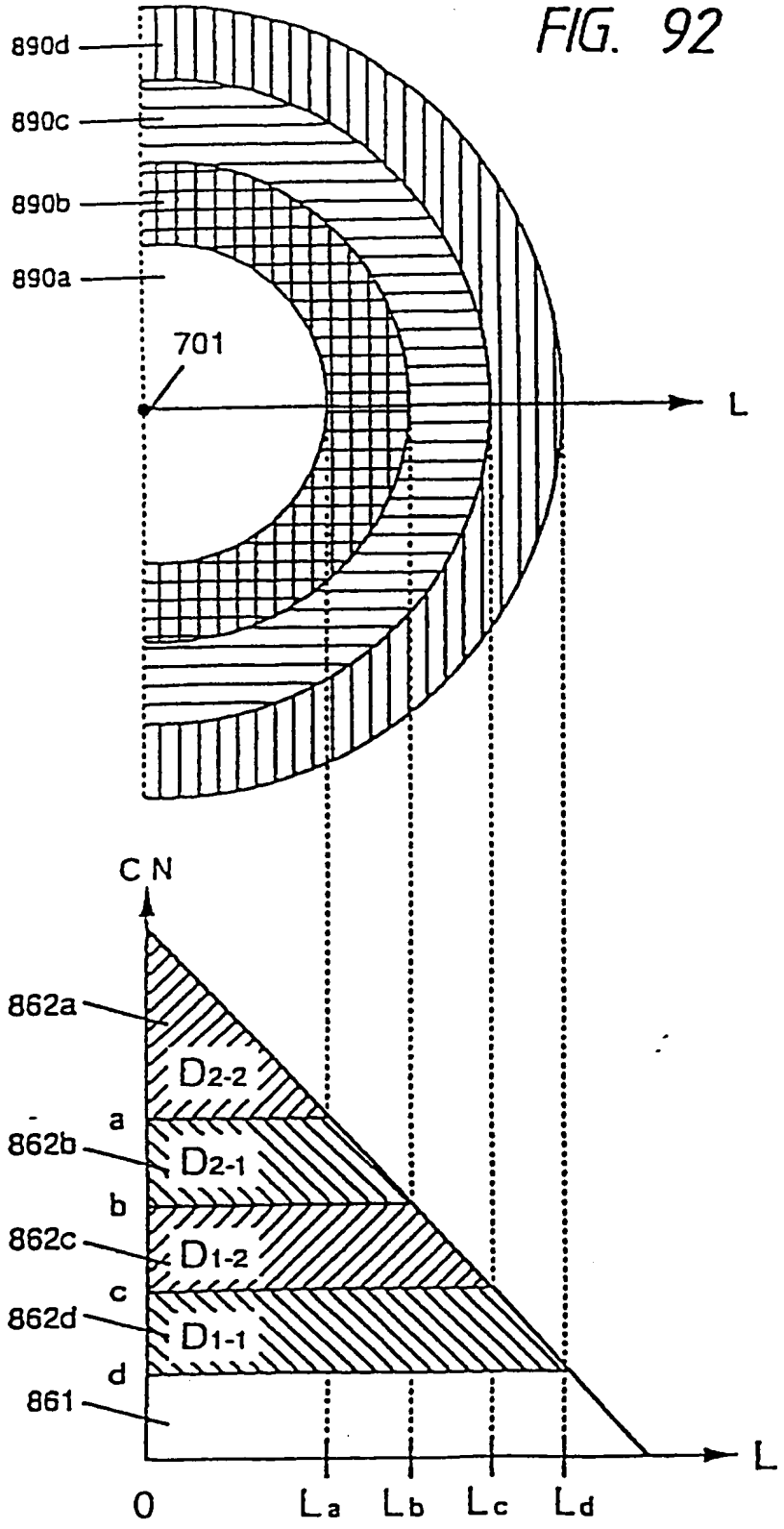

890d
890c
890b
890a
701
L
C N
862a
D2-2
a
862b
D2-1
b
862c
D1-2
c
862d
D1-1
d
861
L
0
La
Lb
Lc
Ld

FIG. 93

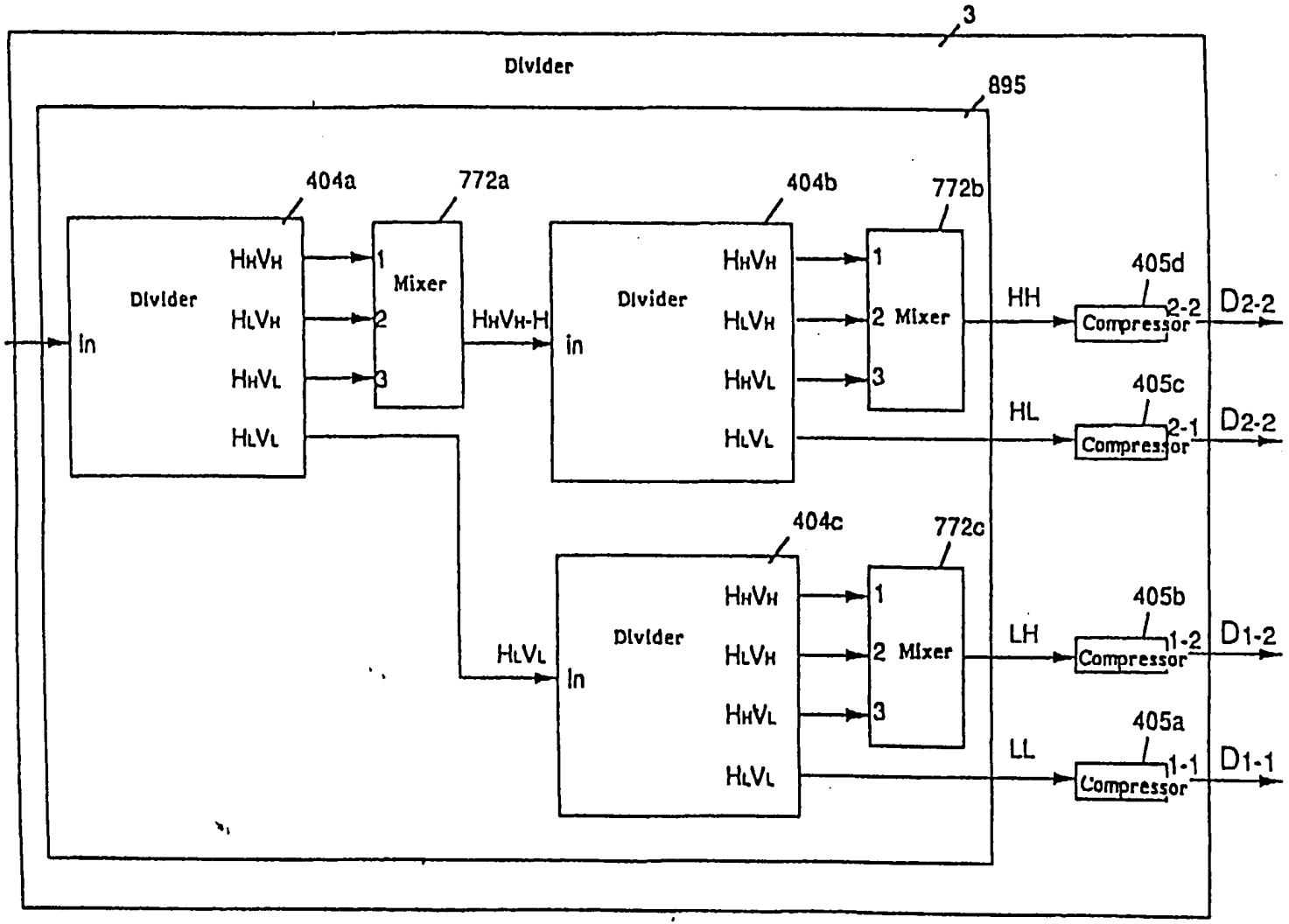

3
Divider
895
404a
772a
404b
772b
405d
405c
405b
405a
Divider
In
HHVH
HLVH
HHVL
HLVL
1
2
3
Mixer
HHVH-H
in
HH
HL
LH
LL
2 Mixer
Compressor
2-2
2-1
1-2
1-1
D2-2
D2-2
D1-2
D1-1
404c
772c
HLVL

FIG. 94

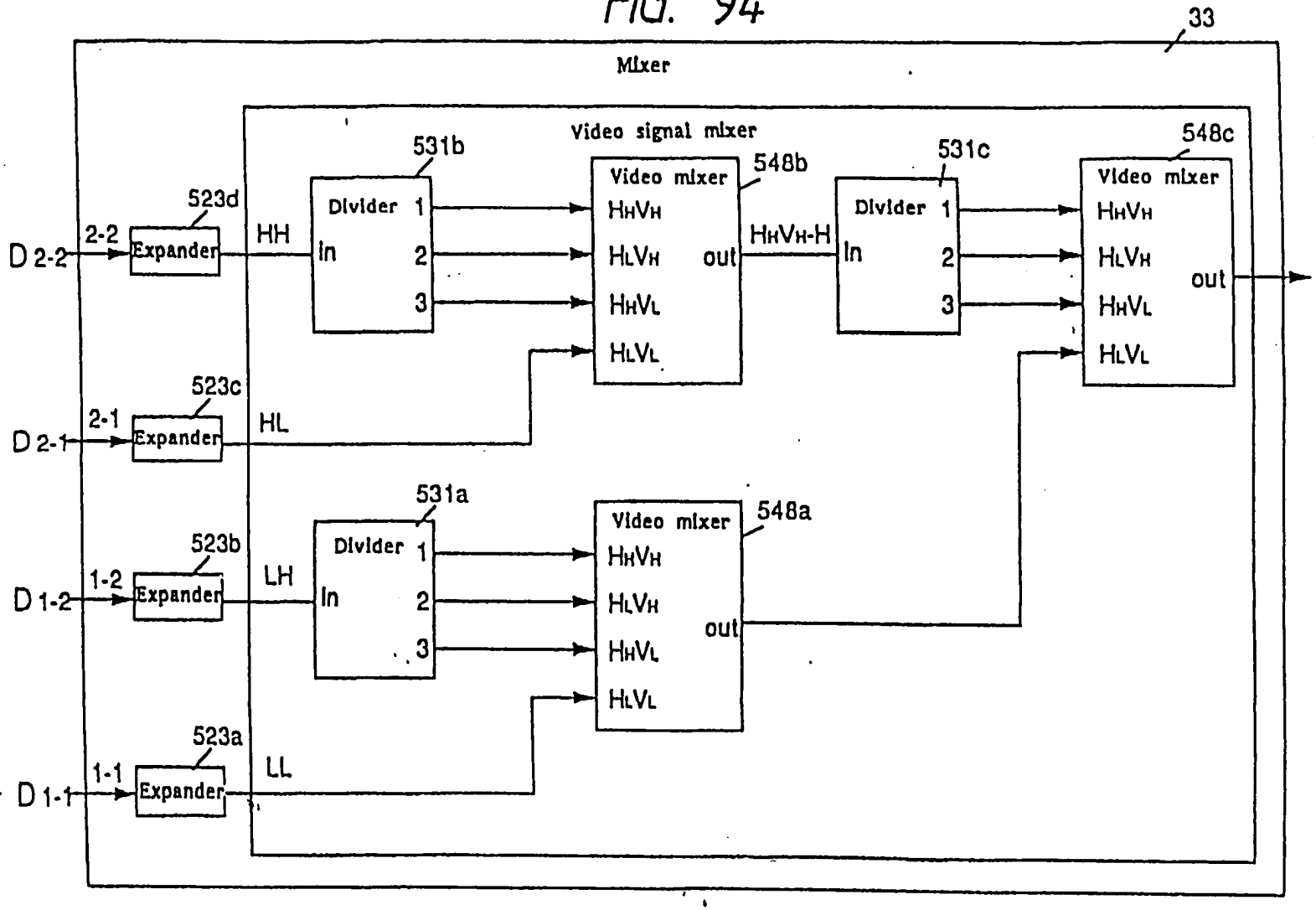

33
Mixer
Video signal mixer
531b
Divider
1
2
3
In
548b
Video mixer
HHVH
HLVH
HHVL
HLVL
out
HHVH-H
531c
Divider
1
2
3
In
548c
Video mixer
HHVH
HLVH
HHVL
HLVL
out
523d
2-2
D 2-2
Expander
HH
523c
2-1
D 2-1
Expander
HL
531a
Divider
1
2
3
In
548a
Video mixer
HHVH
HLVH
HHVL
HLVL
out
523b
1-2
D 1-2
Expander
LH
523a
1-1
D 1-1
Expander
LL

FIG. 95

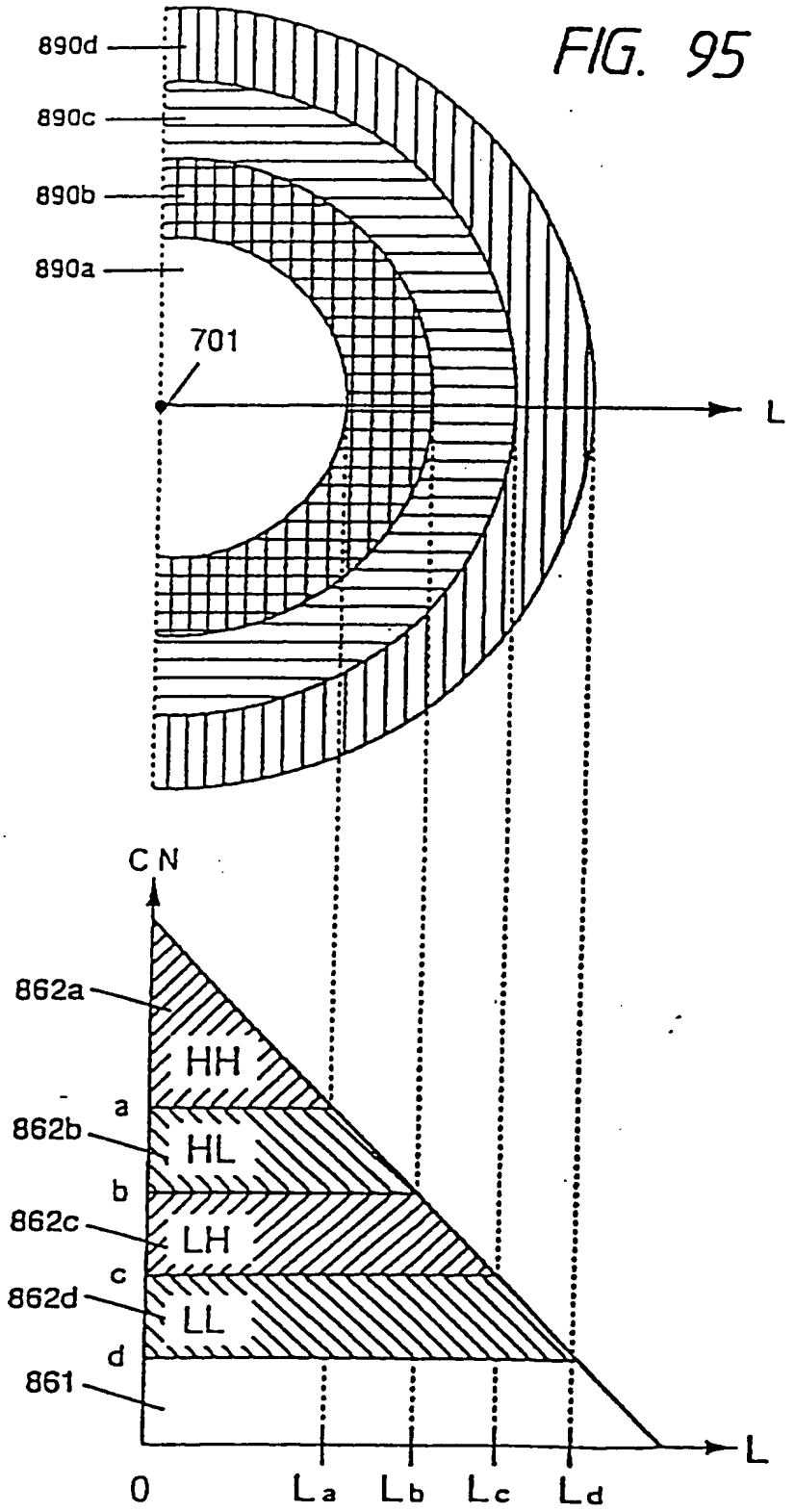

890d
890c
890b
890a
701
L
C N
862a
HH
a
862b
HL
b
862c
LH
c
862d
LL
d
861
L
0
La
Lb
Lc
Ld

FIG. 96

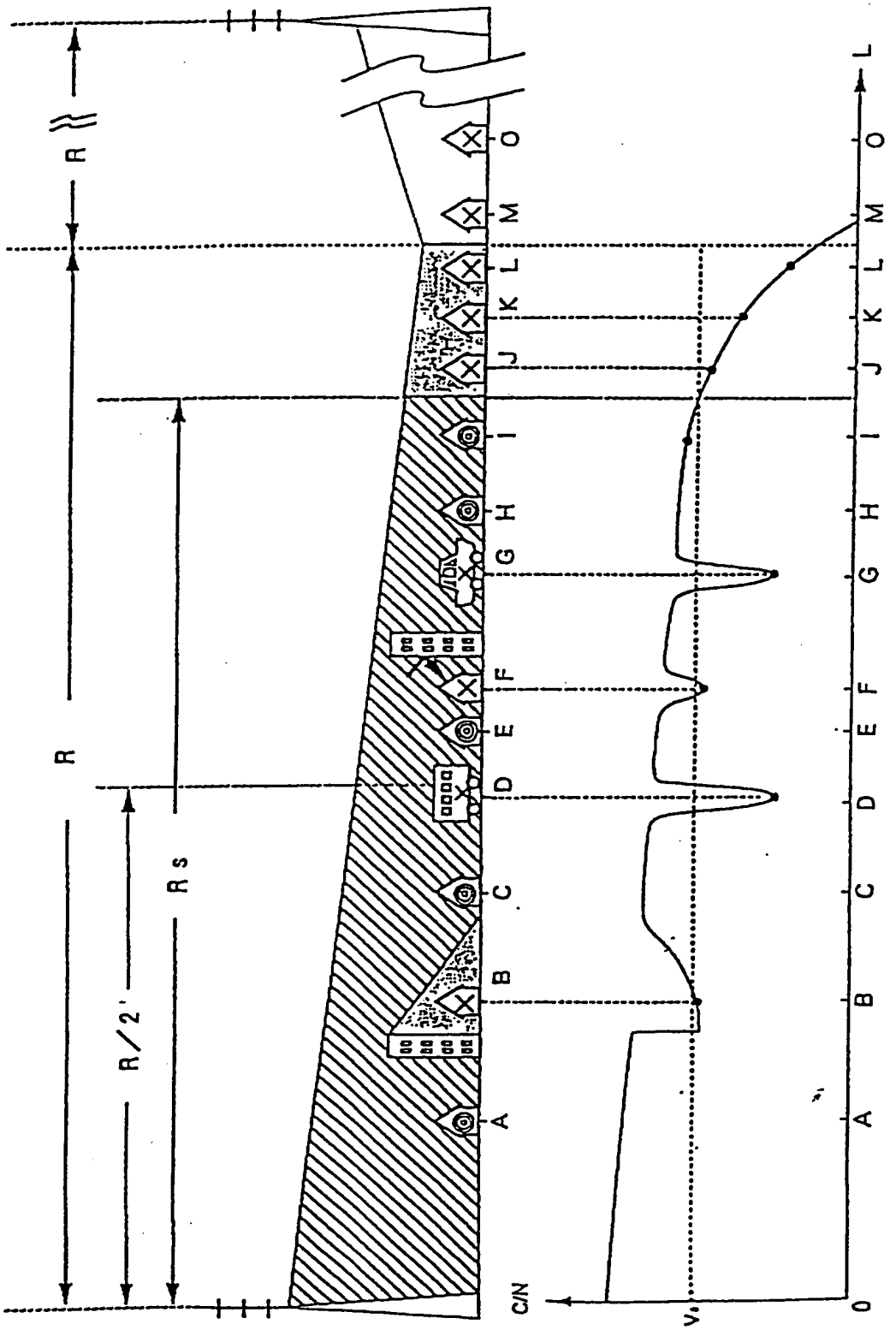


FIG. 97

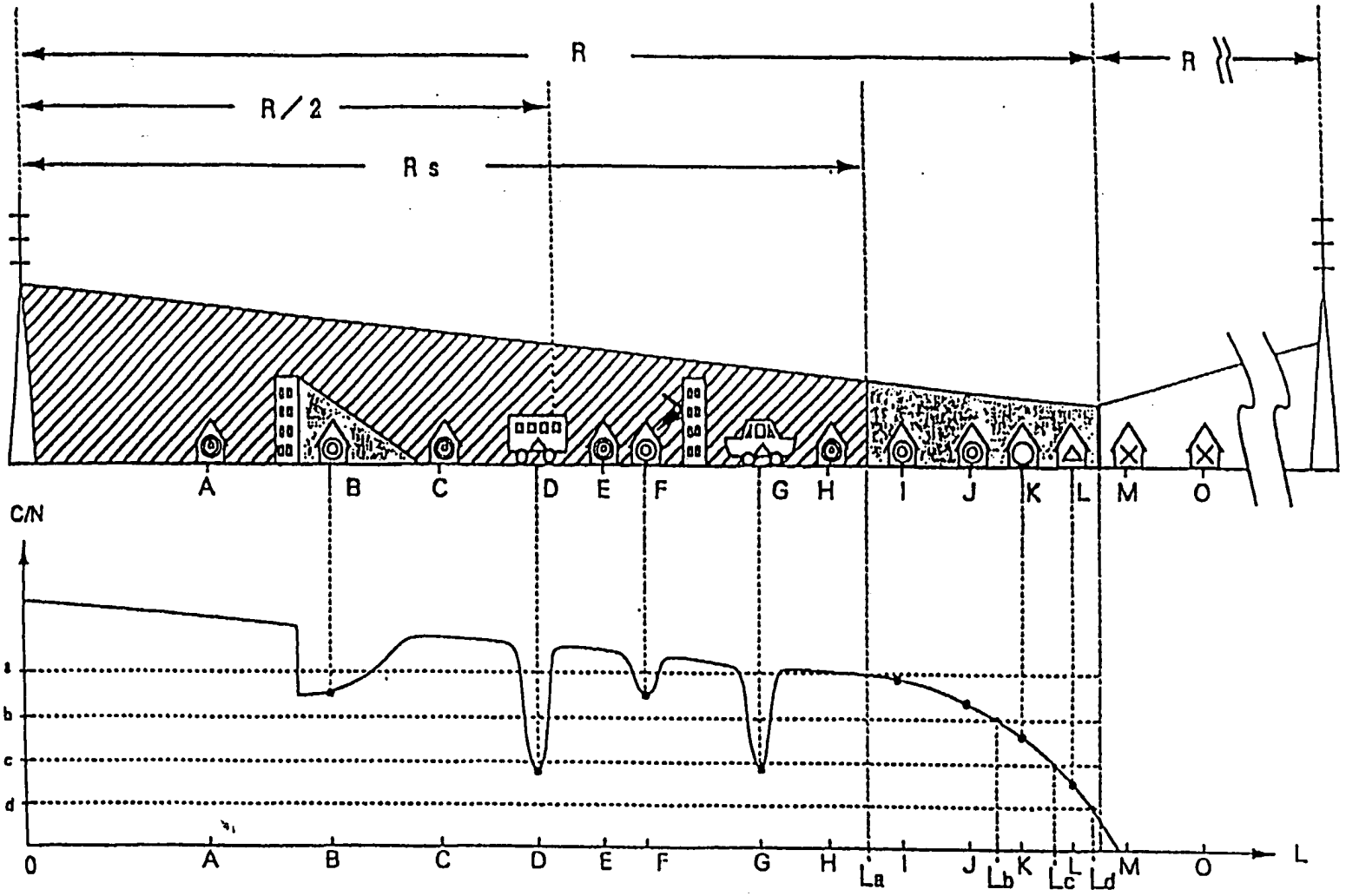

R
R
R/2
Rs
A
B
C
D
E
F
G
H
I
J
K
L
M
O
C/N
a
b
c
d
0
A
B
C
D
E
F
G
H
La
I
J
Lb
K
Lc
L
Ld
M
O
L

FIG. 98

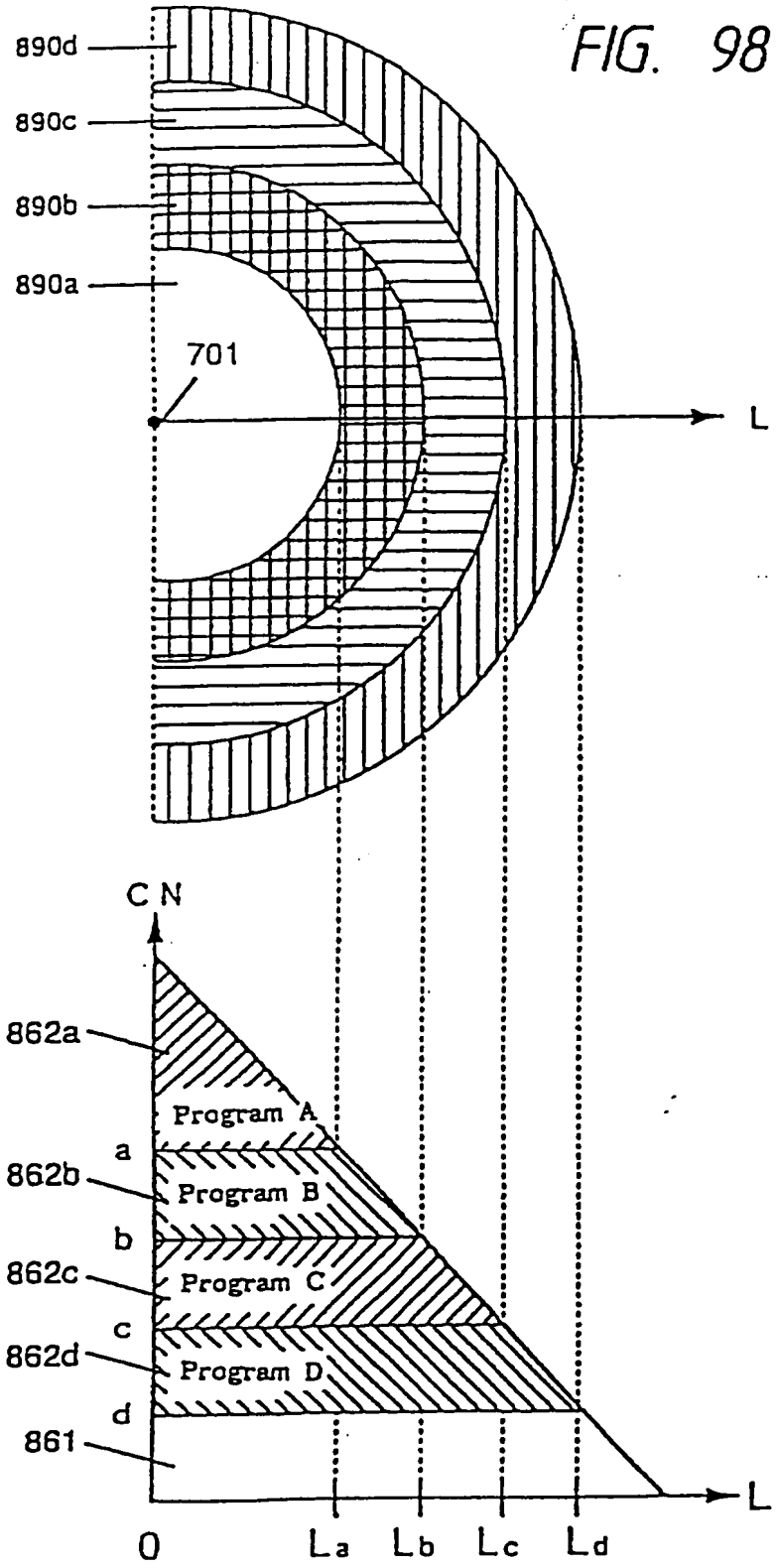

890d
890c
890b
890a
701
L
C N
862a
Program A
a
862b
Program B
b
862c
Program C
c
862d
Program D
d
861
L
0
La
Lb
Lc
Ld

FIG. 99

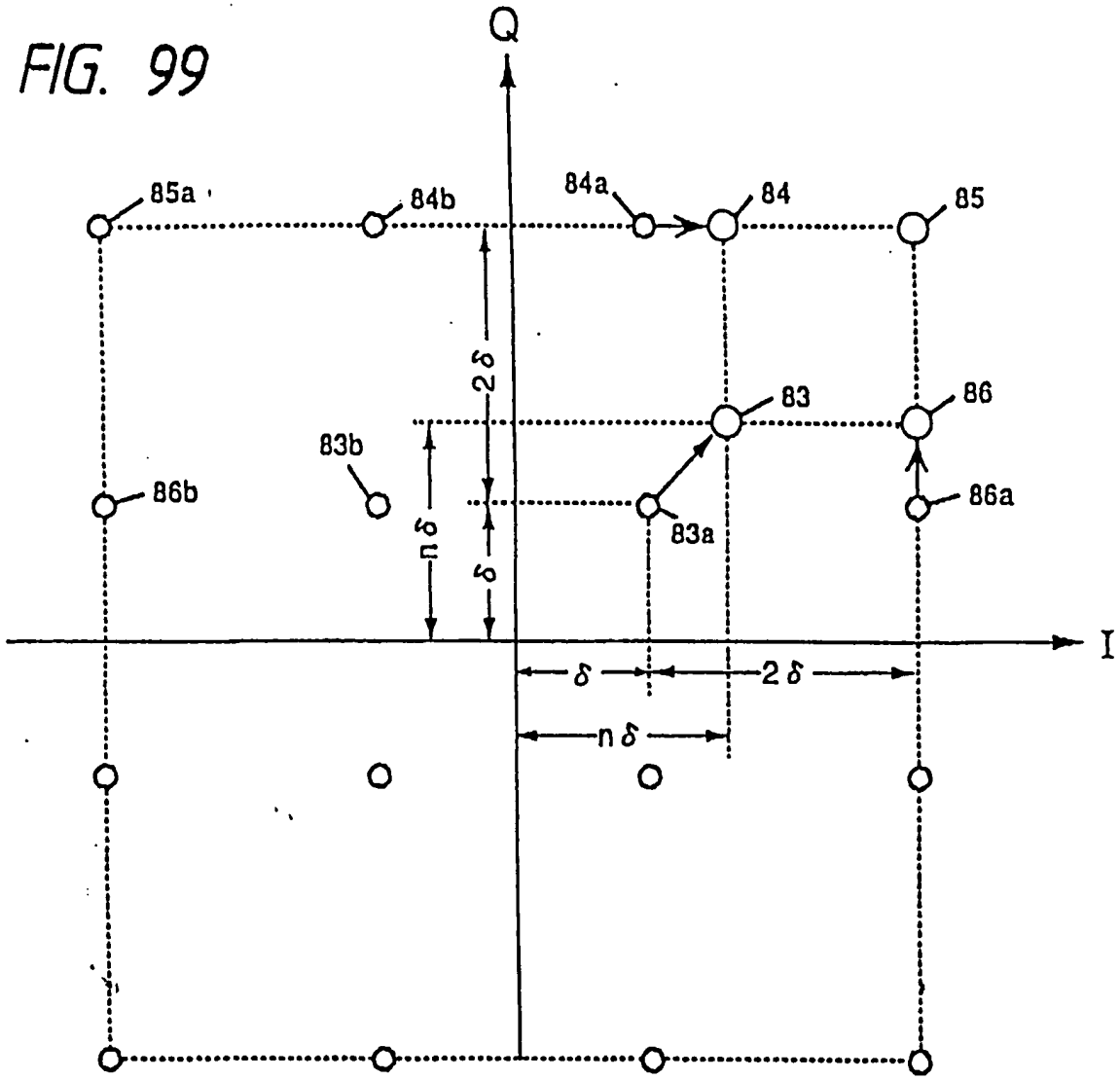


FIG. 100

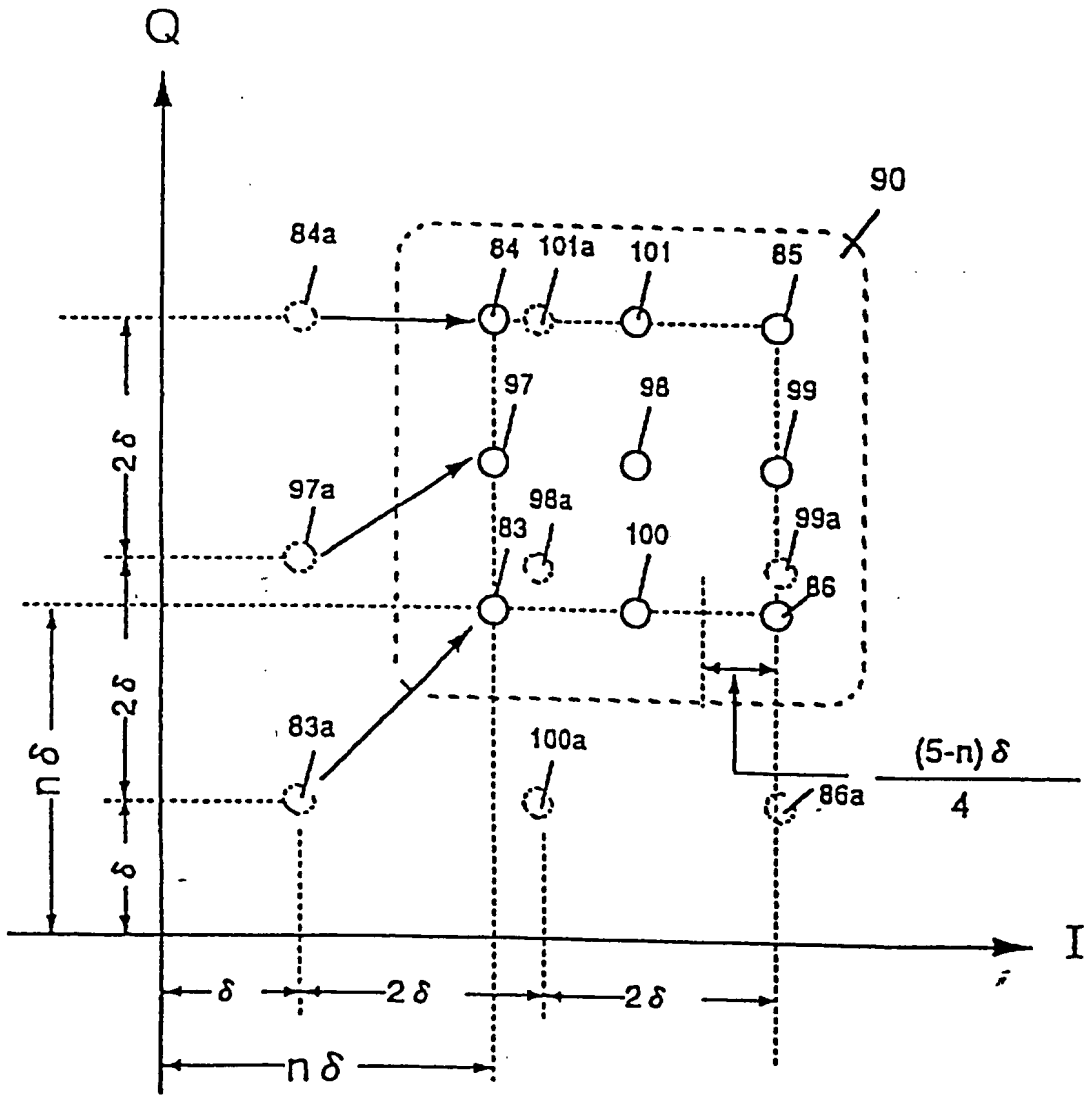

Q
I
90
84a
84
101a
101
85
97
98
99
97a
98a
99a
83
100
86
83a
100a
86a
2δ
2δ
nδ
δ
δ
2δ
2δ
nδ
(5-n) δ
4

FIG. 101

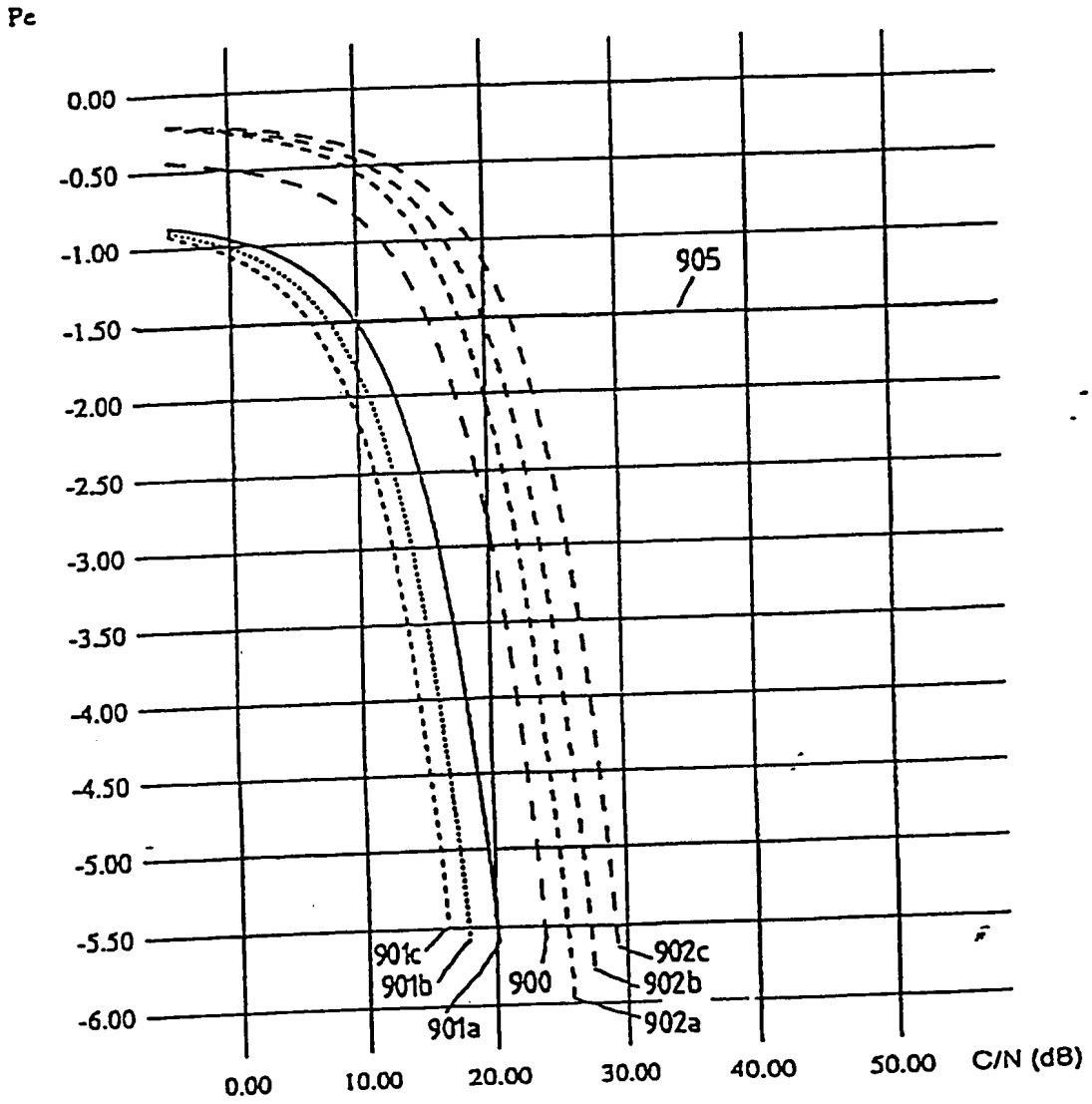

Pe
0.00
-0.50
-1.00
-1.50
-2.00
-2.50
-3.00
-3.50
-4.00
-4.50
-5.00
-5.50
-6.00
905
901c
901b
901a
900
902c
902b
902a
0.00
10.00
20.00
30.00
40.00
50.00
C/N (dB)

FIG. 102

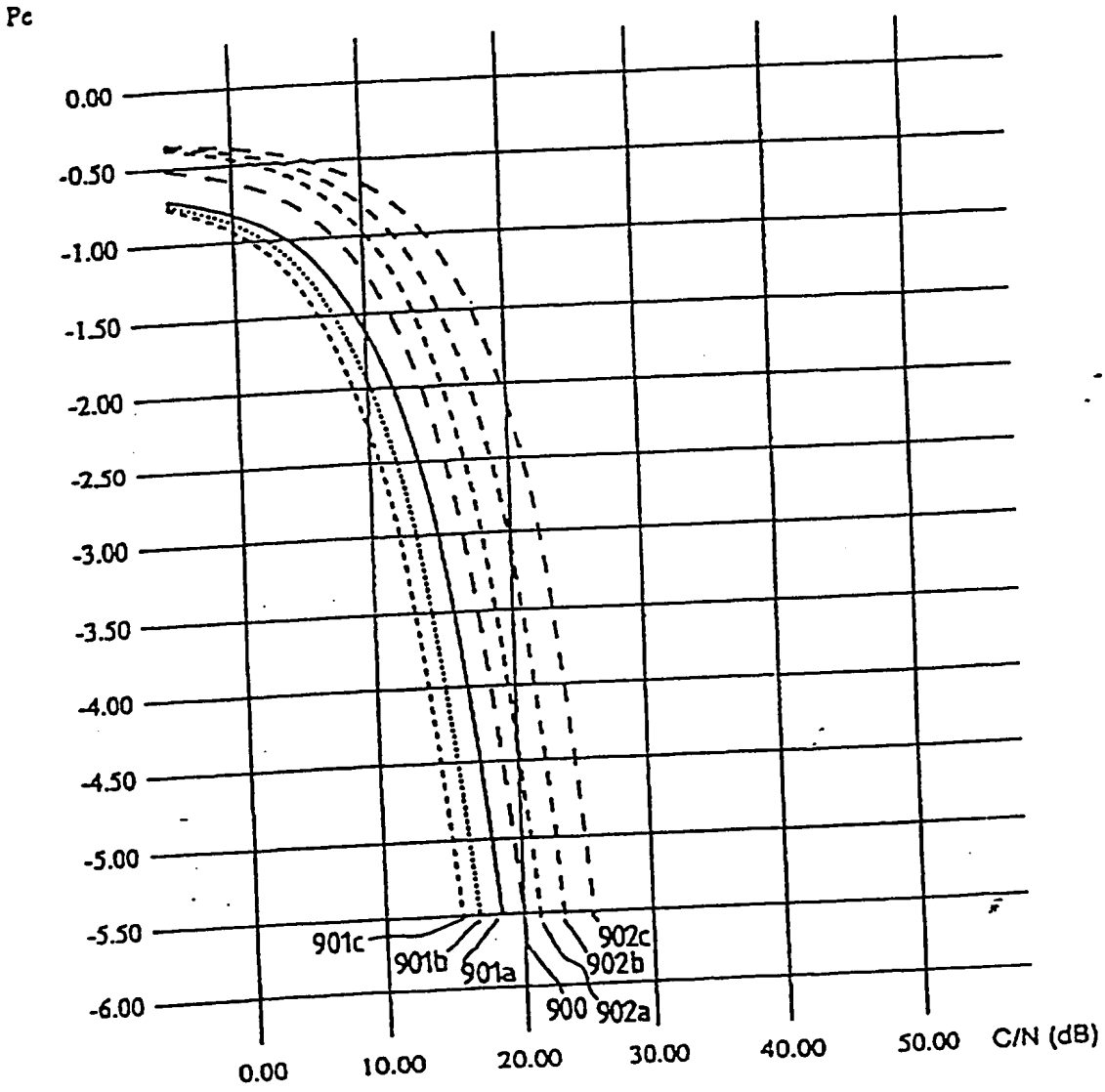

Pc
0.00
-0.50
-1.00
-1.50
-2.00
-2.50
-3.00
-3.50
-4.00
-4.50
-5.00
-5.50
-6.00
0.00
10.00
20.00
30.00
40.00
50.00
C/N (dB)
901c
901b
901a
900
902a
902b
902c

FIG. 103

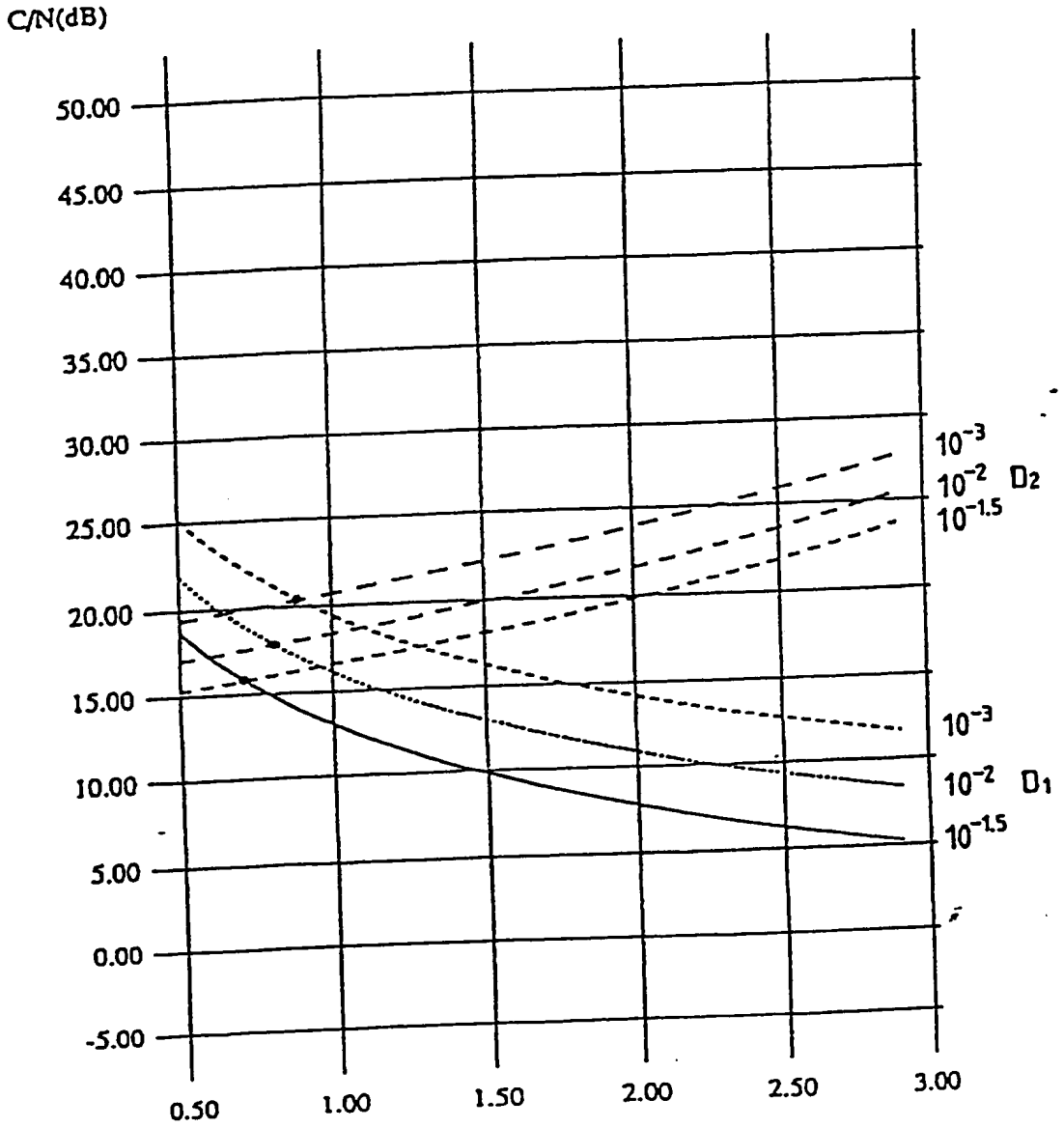

C/N(dB)
50.00
45.00
40.00
35.00
30.00
25.00
20.00
15.00
10.00
5.00
0.00
-5.00
0.50
1.00
1.50
2.00
2.50
3.00
10^{-3}
10^{-2} D2
$10^{-1.5}$
10^{-3}
10^{-2} D1
$10^{-1.5}$

FIG. 104

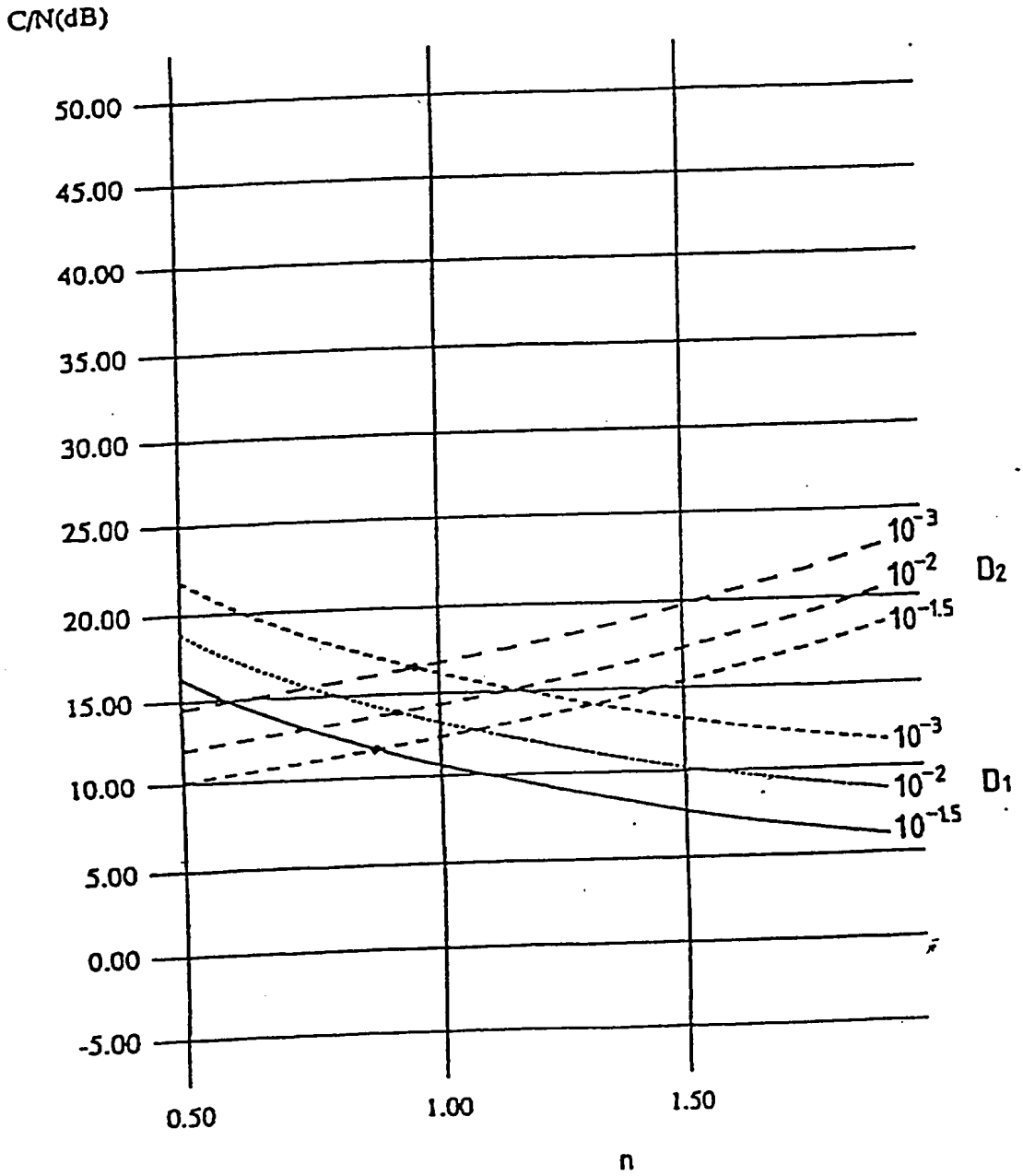

C/N(dB)
50.00
45.00
40.00
35.00
30.00
25.00
20.00
15.00
10.00
5.00
0.00
-5.00
0.50
1.00
1.50
n
10^{-3}
10^{-2}
$10^{-1.5}$
D_2
10^{-3}
10^{-2}
$10^{-1.5}$
D_1

FIG. 105

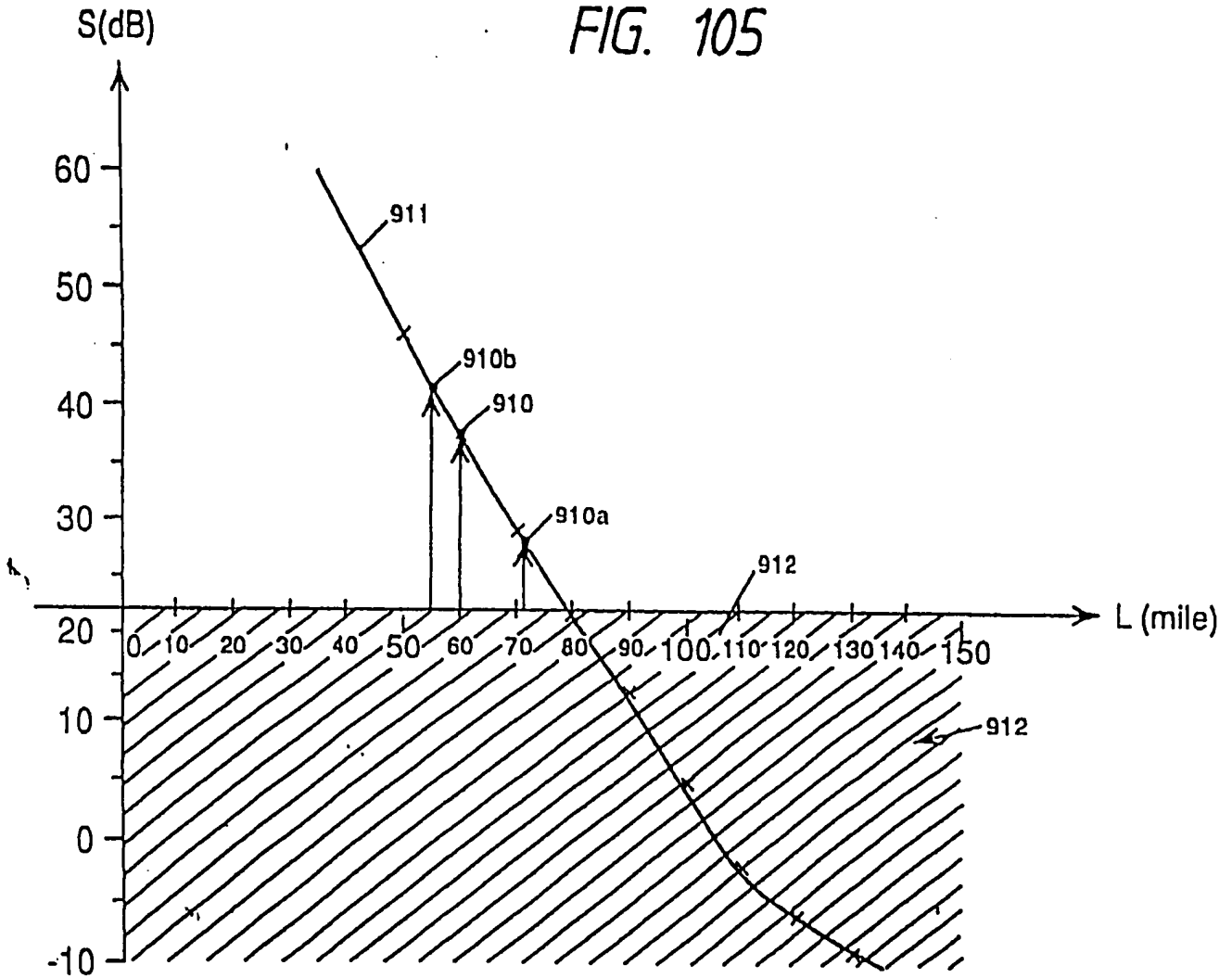

S(dB)
60
50
40
30
20
10
0
-10
911
910b
910
910a
912
912
L (mile)
0
10
20
30
40
50
60
70
80
90
100
110
120
130
140
150

FIG. 106

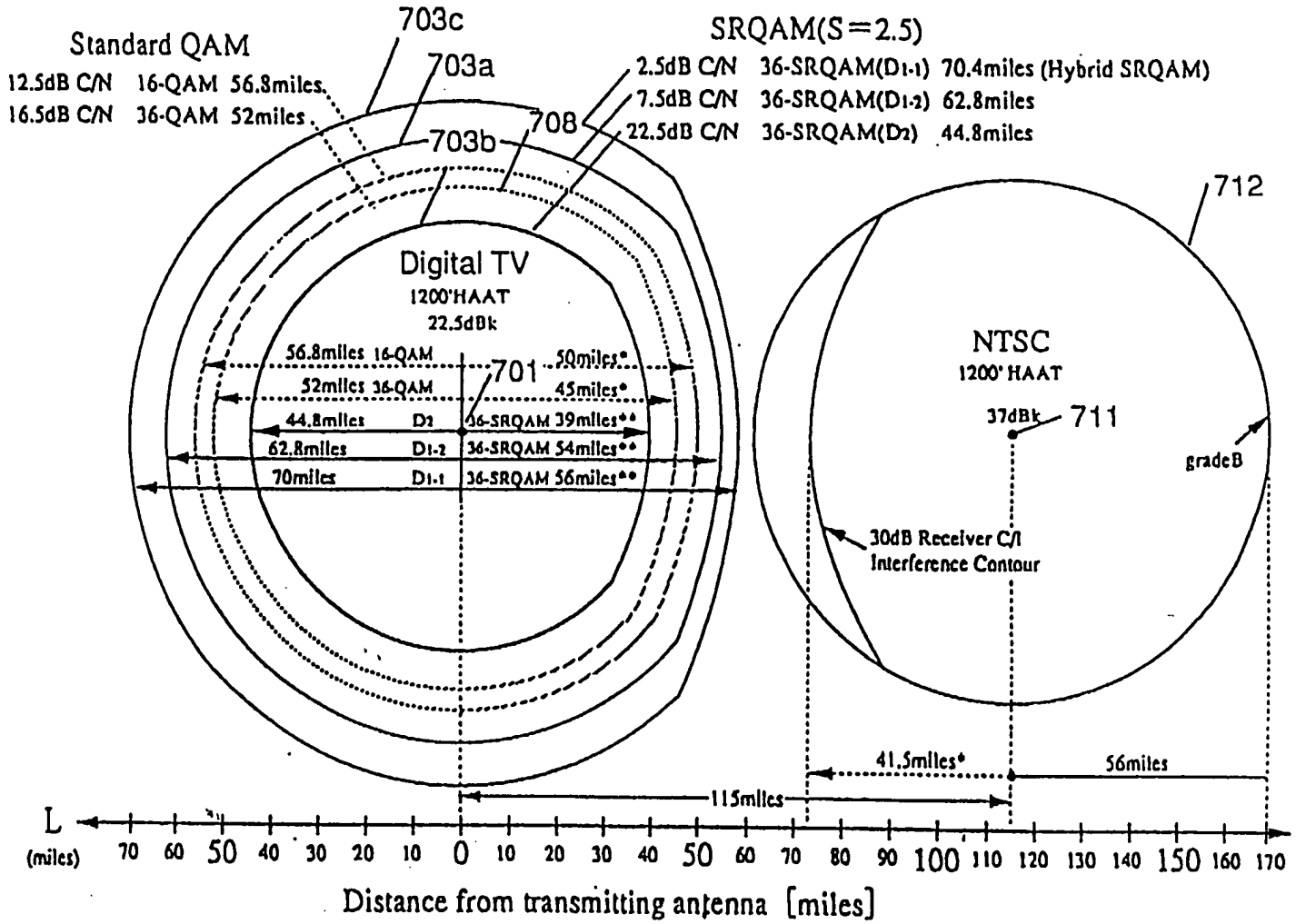

Standard QAM
12.5dB C/N 16-QAM 56.8miles
16.5dB C/N 36-QAM 52miles
703c
703a
703b
708
SRQAM(S=2.5)
2.5dB C/N 36-SRQAM(D1-1) 70.4miles (Hybrid SRQAM)
7.5dB C/N 36-SRQAM(D1-2) 62.8miles
22.5dB C/N 36-SRQAM(D2) 44.8miles
712
Digital TV
1200'HAAT
22.5dBk
56.8miles 16-QAM
52miles 36-QAM
44.8miles D2
62.8miles D1-2
70miles D1-1
701
50miles*
45miles*
36-SRQAM 39miles**
36-SRQAM 54miles**
36-SRQAM 56miles**
NTSC
1200' HAAT
37dBk
711
gradeB
30dB Receiver C/I
Interference Contour
41.5miles*
56miles
115miles
L
(miles)
70 60 50 40 30 20 10 0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170
Distance from transmitting antenna [miles]

FIG. 107

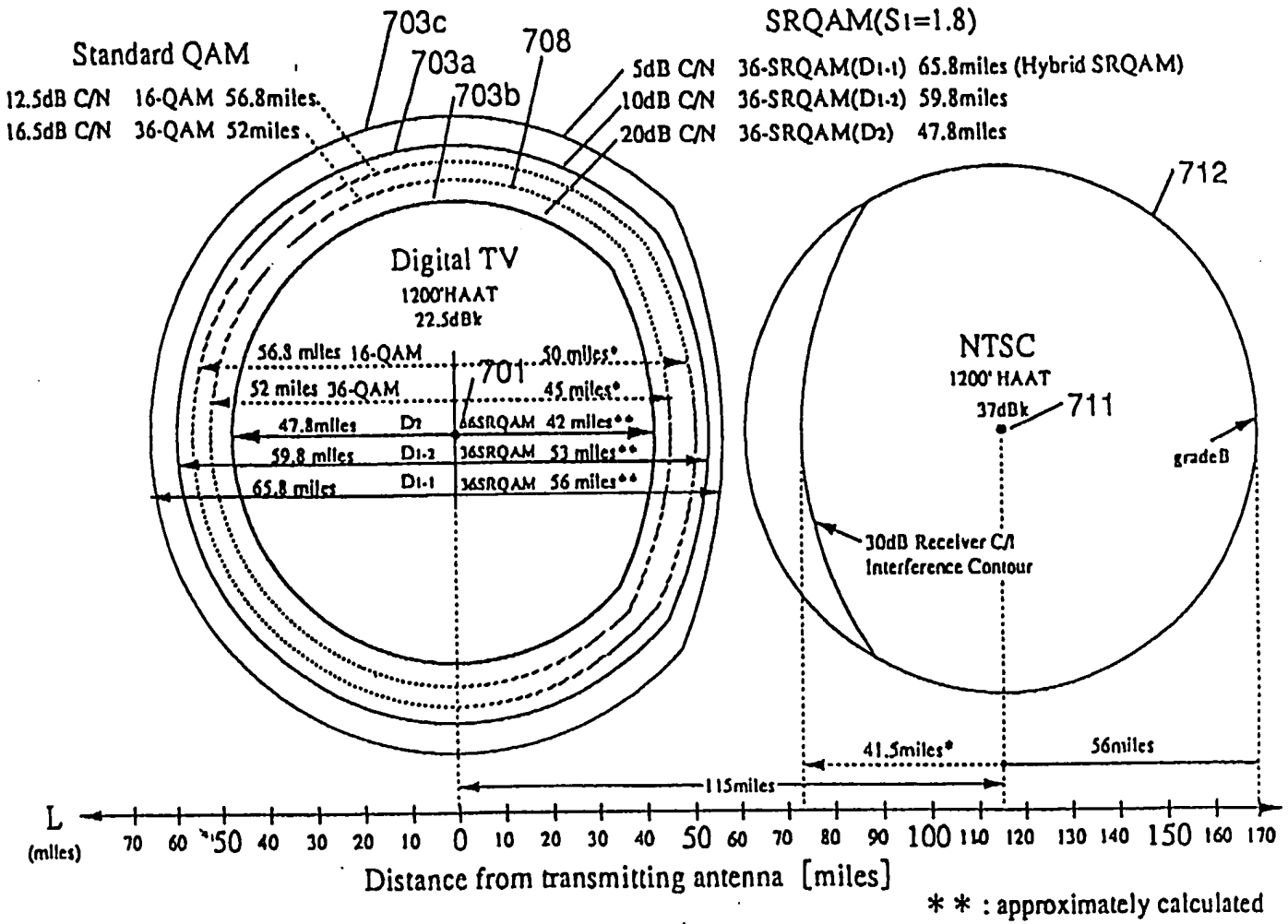

Standard QAM
12.5dB C/N 16-QAM 56.8miles
16.5dB C/N 36-QAM 52miles
703c
703a
703b
708
SRQAM(S1=1.8)
5dB C/N 36-SRQAM(D1-1) 65.8miles (Hybrid SRQAM)
10dB C/N 36-SRQAM(D1-2) 59.8miles
20dB C/N 36-SRQAM(D2) 47.8miles
712
Digital TV
1200'HAAT
22.5dBk
56.8 miles 16-QAM
50 miles*
52 miles 36-QAM
45 miles*
701
47.8miles D2 36SRQAM 42 miles**
59.8 miles D1-2 36SRQAM 53 miles**
65.8 miles D1-1 36SRQAM 56 miles**
NTSC
1200' HAAT
37dBk
711
gradeB
30dB Receiver C/I
Interference Contour
41.5miles*
56miles
115miles
L
(miles)
70 60 50 40 30 20 10 0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170
Distance from transmitting antenna [miles]
* * : approximately calculated

FIG. 108(a)

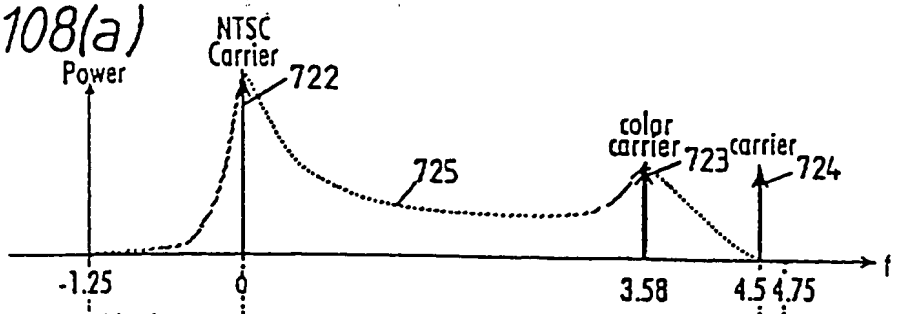


FIG. 108(b)

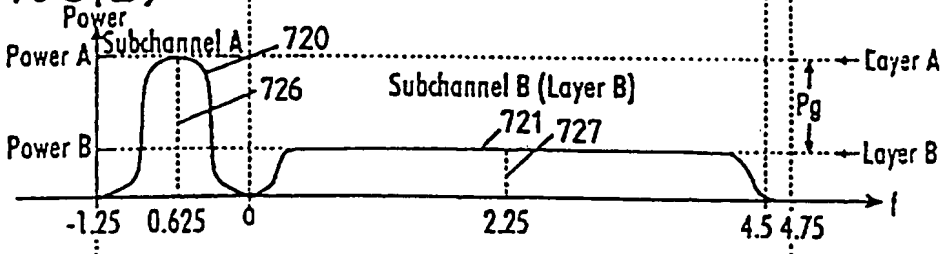


FIG. 108(c)

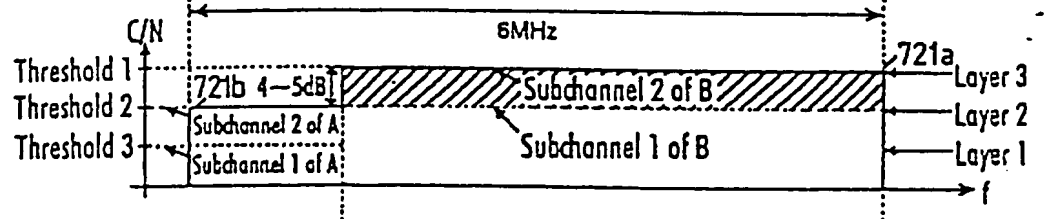


FIG. 108(d)

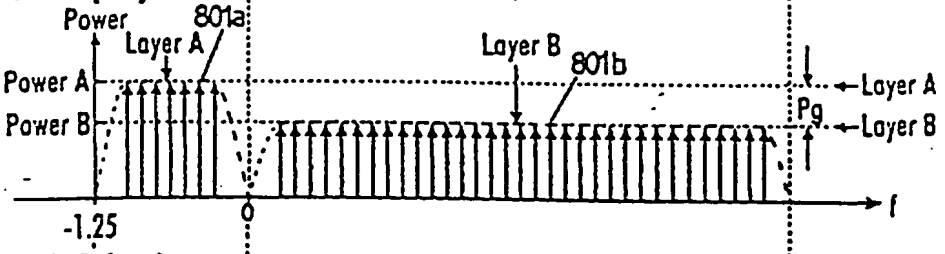


FIG. 108(e)

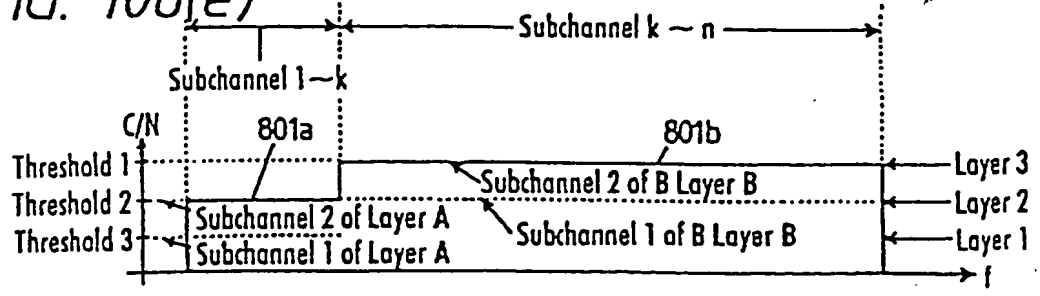


FIG. 109

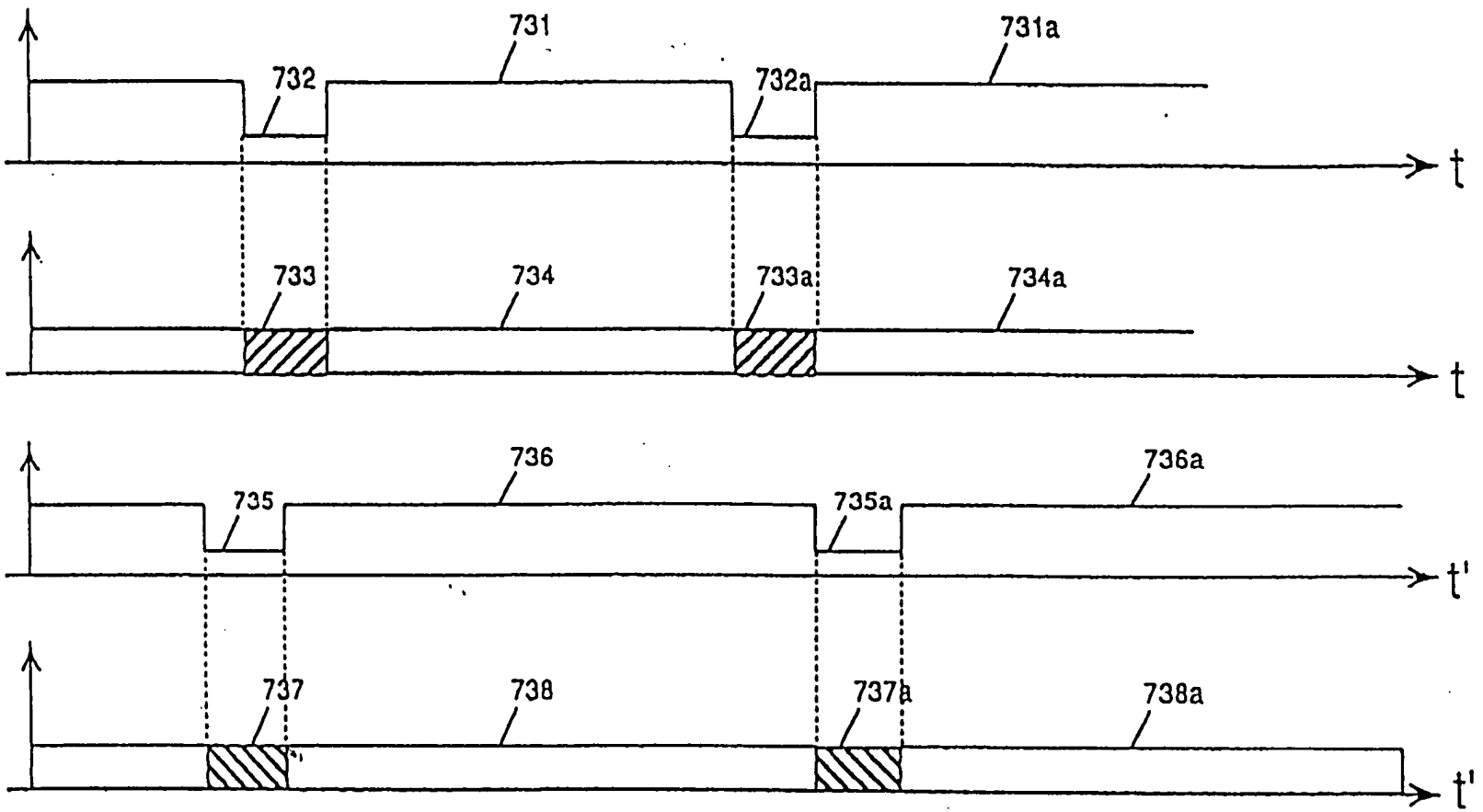

731
731a
732
732a
t
733
734
733a
734a
t
736
736a
735
735a
t'
737
738
737a
738a
t'

FIG. 110

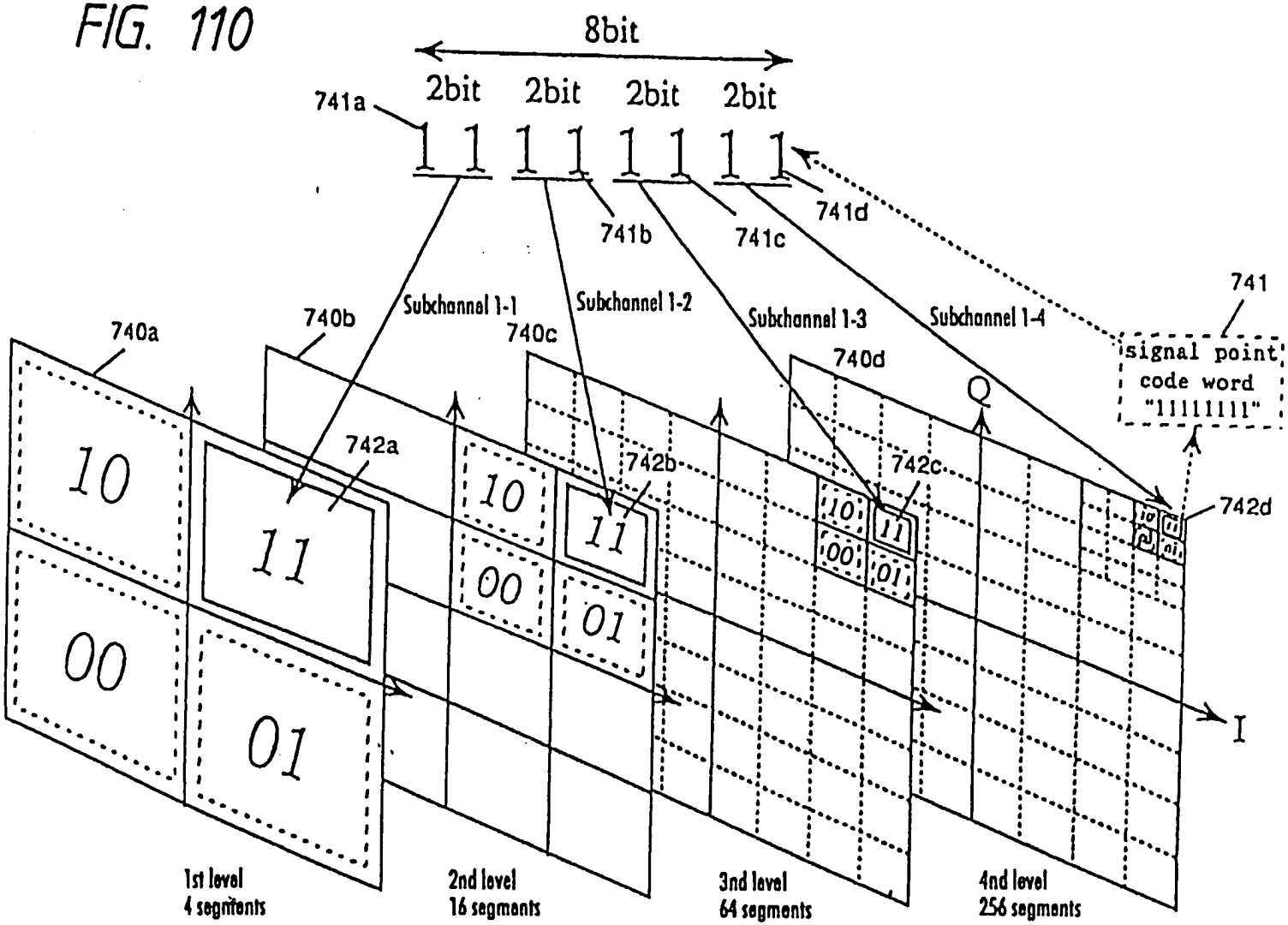

8bit
2bit 2bit 2bit 2bit
741a
1 1 1 1 1 1 1 1
741b
741c
741d
741
signal point
code word
"11111111"
740a
740b
740c
740d
Subchannel 1-1
Subchannel 1-2
Subchannel 1-3
Subchannel 1-4
742a
742b
742c
742d
Q
I
10
11
00
01
1st level
4 segments
2nd level
16 segments
3nd level
64 segments
4nd level
256 segments

FIG. 111

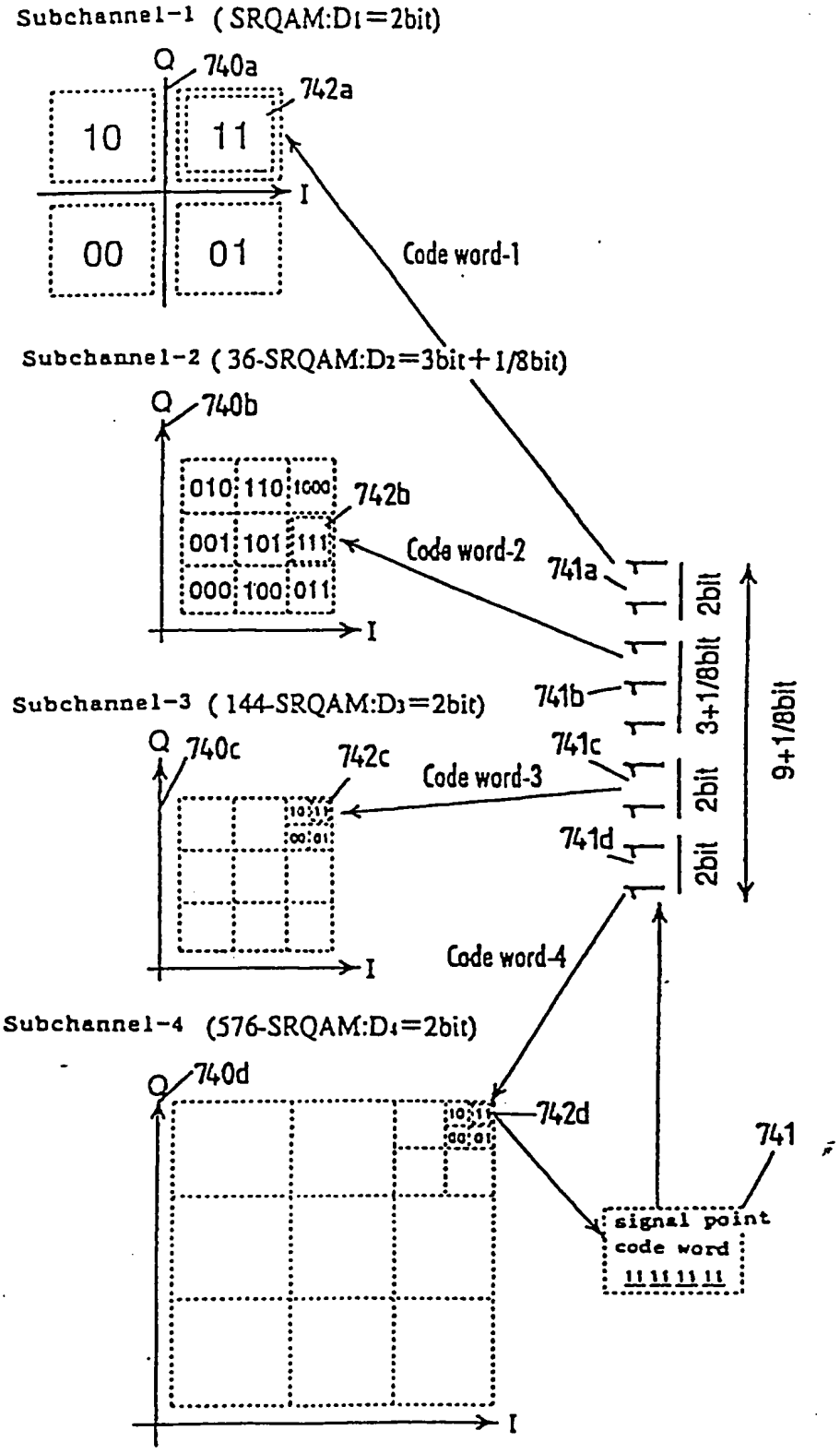

Subchannel-1 (SRQAM:D1=2bit)
Q
740a
742a
10
11
00
01
I
Code word-1
Subchannel-2 (36-SRQAM:D2=3bit+1/8bit)
740b
742b
010 110 1000
001 101 111
000 100 011
Code word-2
741a
741b
741c
741d
2bit
3+1/8bit
2bit
2bit
9+1/8bit
Subchannel-3 (144-SRQAM:D3=2bit)
740c
742c
Code word-3
Code word-4
Subchannel-4 (576-SRQAM:D4=2bit)
740d
742d
741
signal point
code word
11 11 11 11

FIG. 112

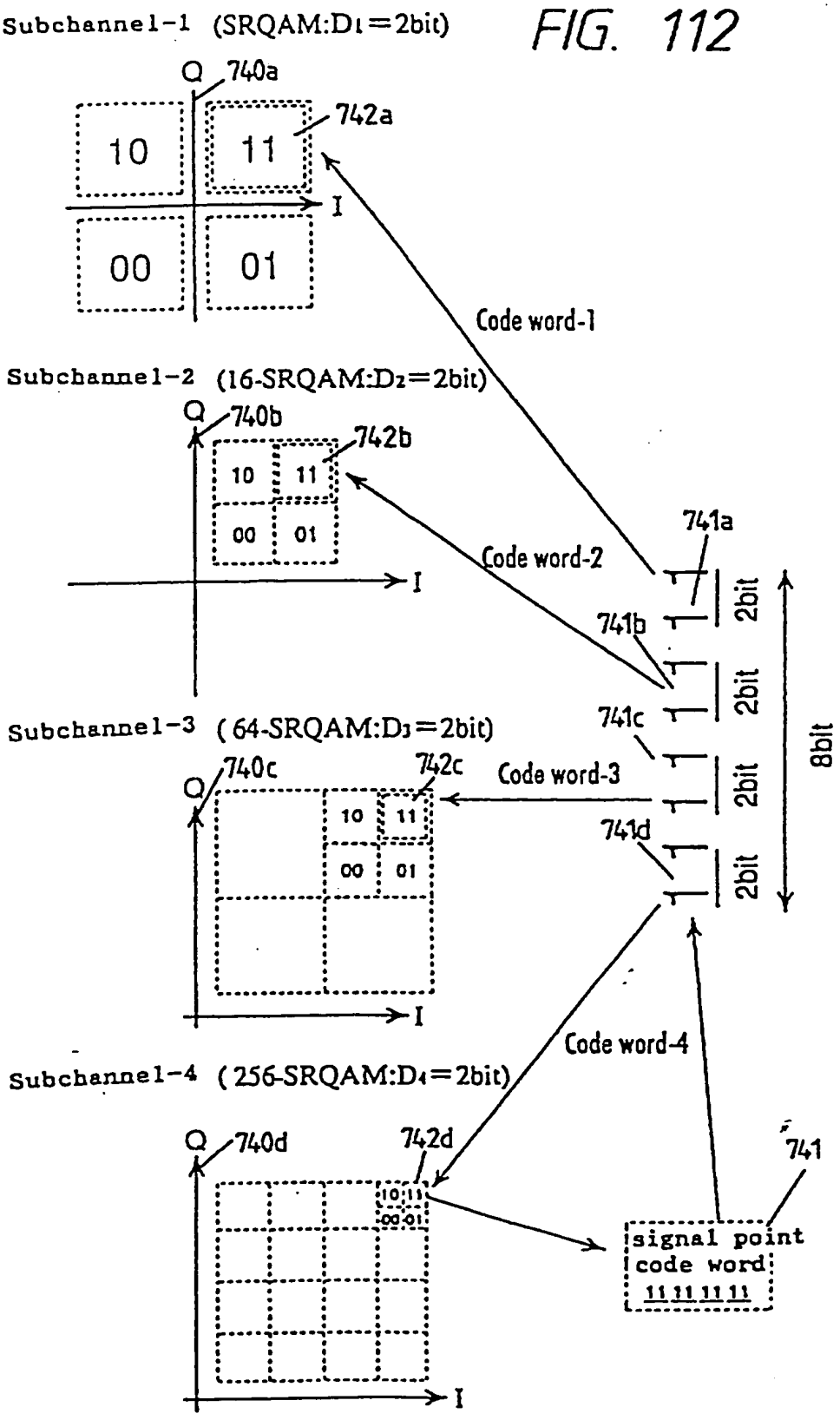

Subchannel-1 (SRQAM:D1=2bit)
Q
740a
742a
10
11
00
01
I
Code word-1
Subchannel-2 (16-SRQAM:D2=2bit)
740b
742b
Code word-2
Subchannel-3 (64-SRQAM:D3=2bit)
740c
742c
Code word-3
Subchannel-4 (256-SRQAM:D4=2bit)
740d
742d
Code word-4
741a
741b
741c
741d
2bit
8bit
741
signal point
code word
11 11 11 11

FIG. 113

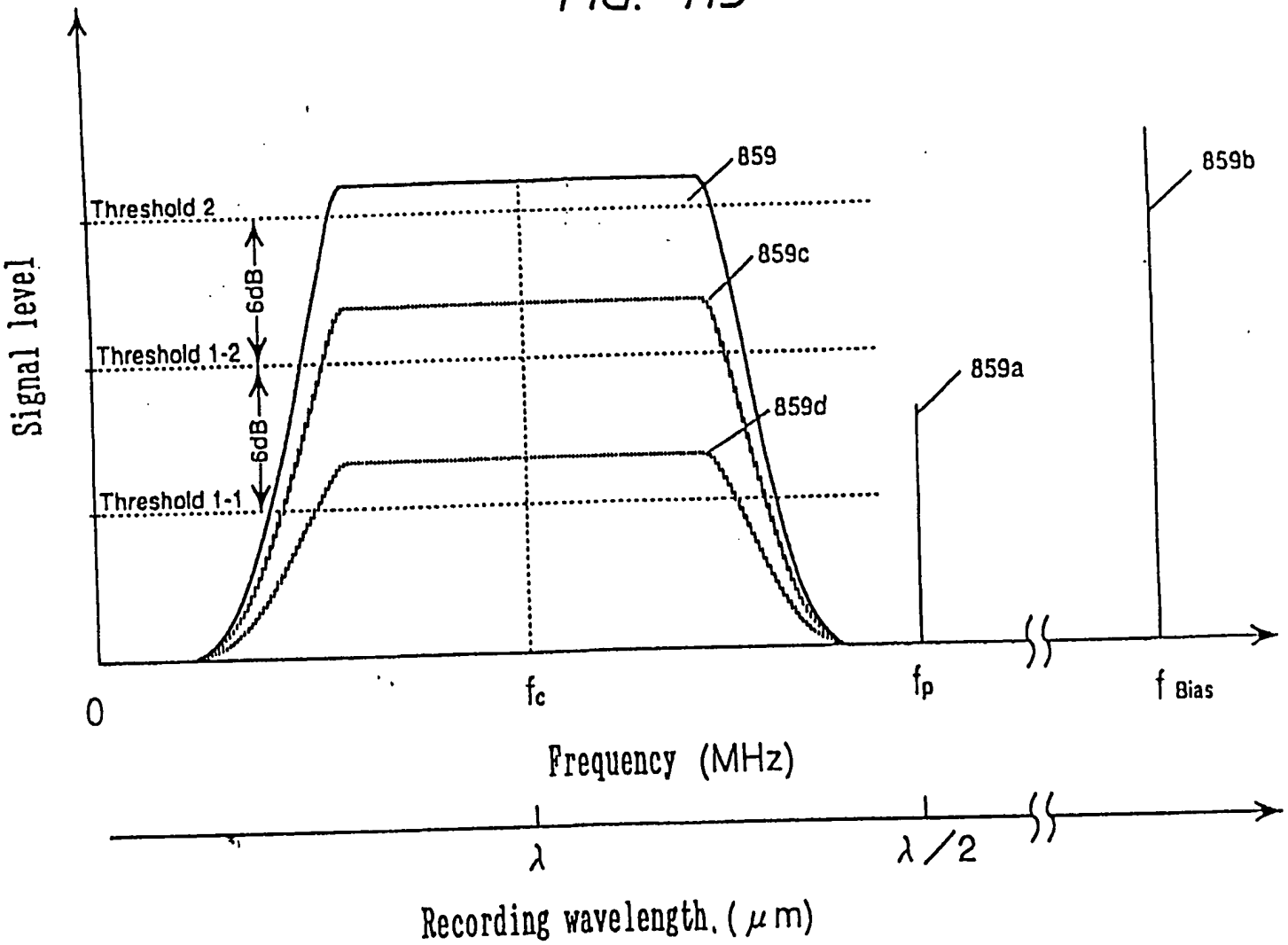

Signal level
Threshold 2
Threshold 1-2
Threshold 1-1
6dB
6dB
859
859c
859d
859a
859b
0
fc
fp
f Bias
Frequency (MHz)
λ
λ/2
Recording wavelength, (μm)

FIG. 114

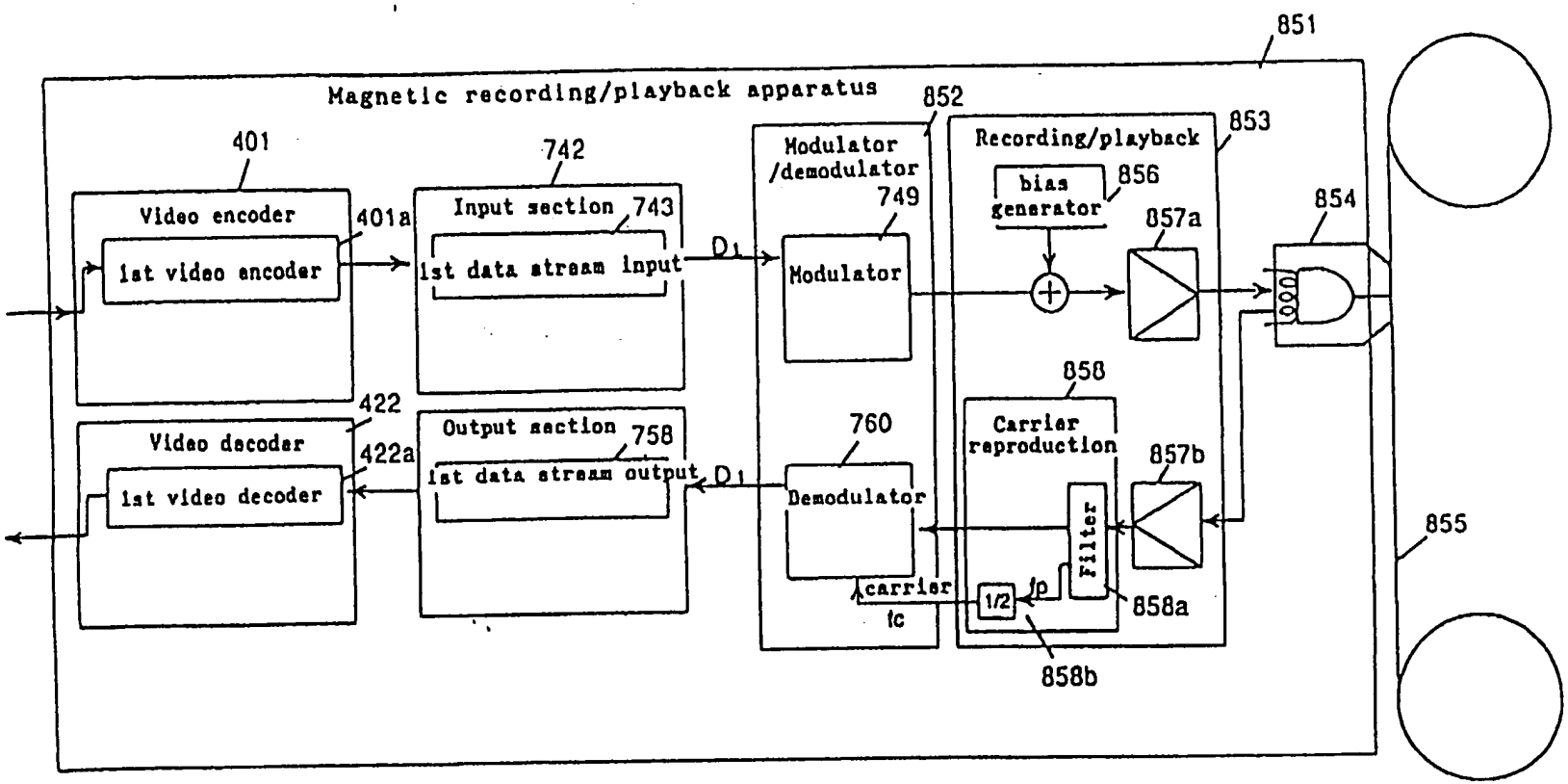

851
Magnetic recording/playback apparatus
852
853
401
742
Modulator /demodulator
Recording/playback
bias generator
856
749
854
Video encoder
401a
Input section
743
1st video encoder
1st data stream input
D1
Modulator
857a
858
422
Output section
758
760
Carrier reproduction
857b
Video decoder
422a
1st video decoder
1st data stream output
D1
Demodulator
855
Filter
carrier
fc
1/2
fp
858a
858b

FIG. 115

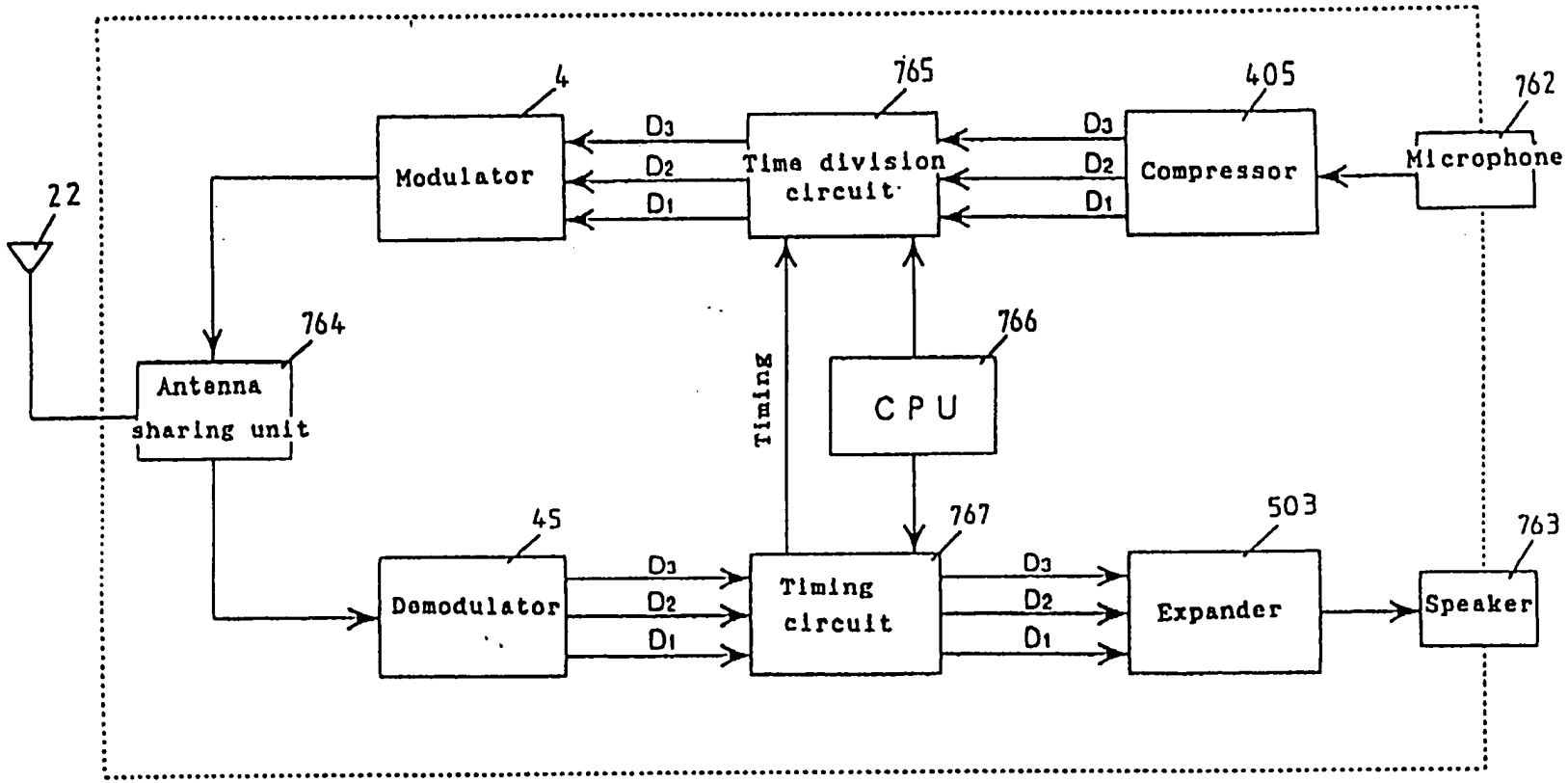

22
4
765
405
762
Modulator
D3
D2
D1
Time division circuit
Compressor
Microphone
764
Antenna sharing unit
Timing
766
CPU
45
767
503
763
Demodulator
Timing circuit
Expander
Speaker

FIG. 116

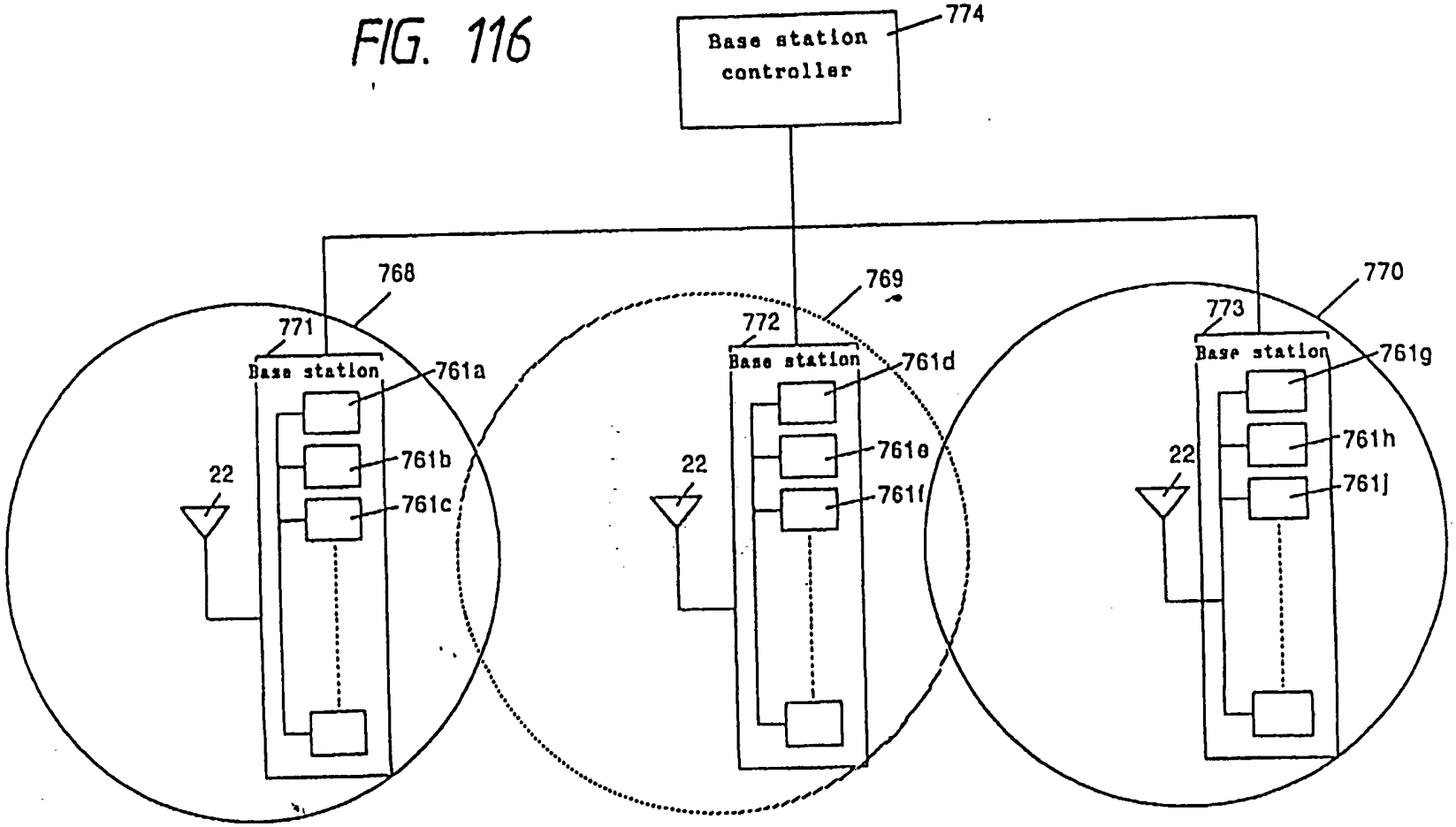

Base station controller
774
768
769
770
771
772
773
Base station
Base station
Base station
761a
761b
761c
761d
761e
761f
761g
761h
761j
22
22
22

FIG. 117

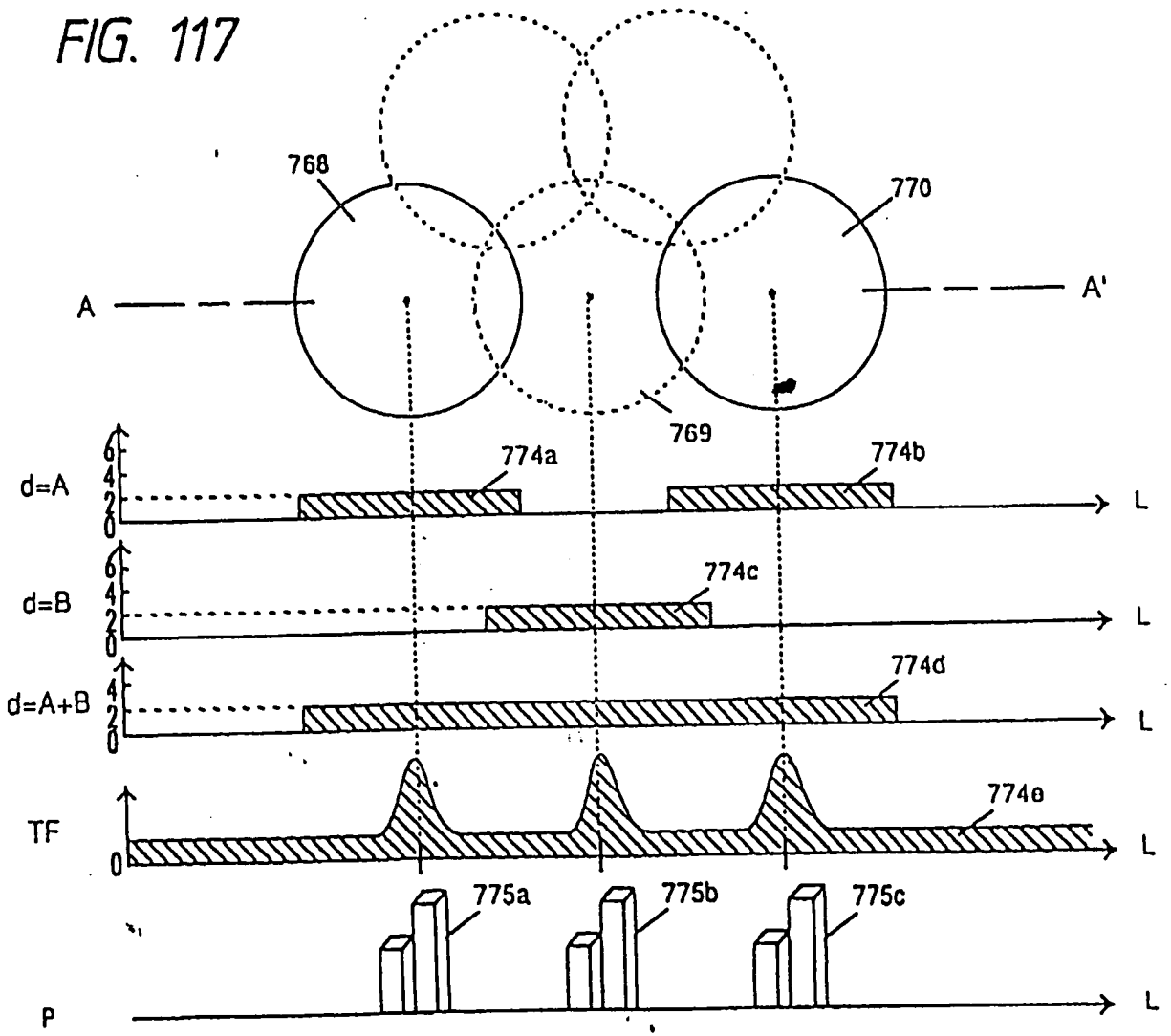

768
770
A
A'
769
d=A
6
4
2
0
774a
774b
L
d=B
774c
d=A+B
774d
TF
774e
775a
775b
775c
P

FIG. 118

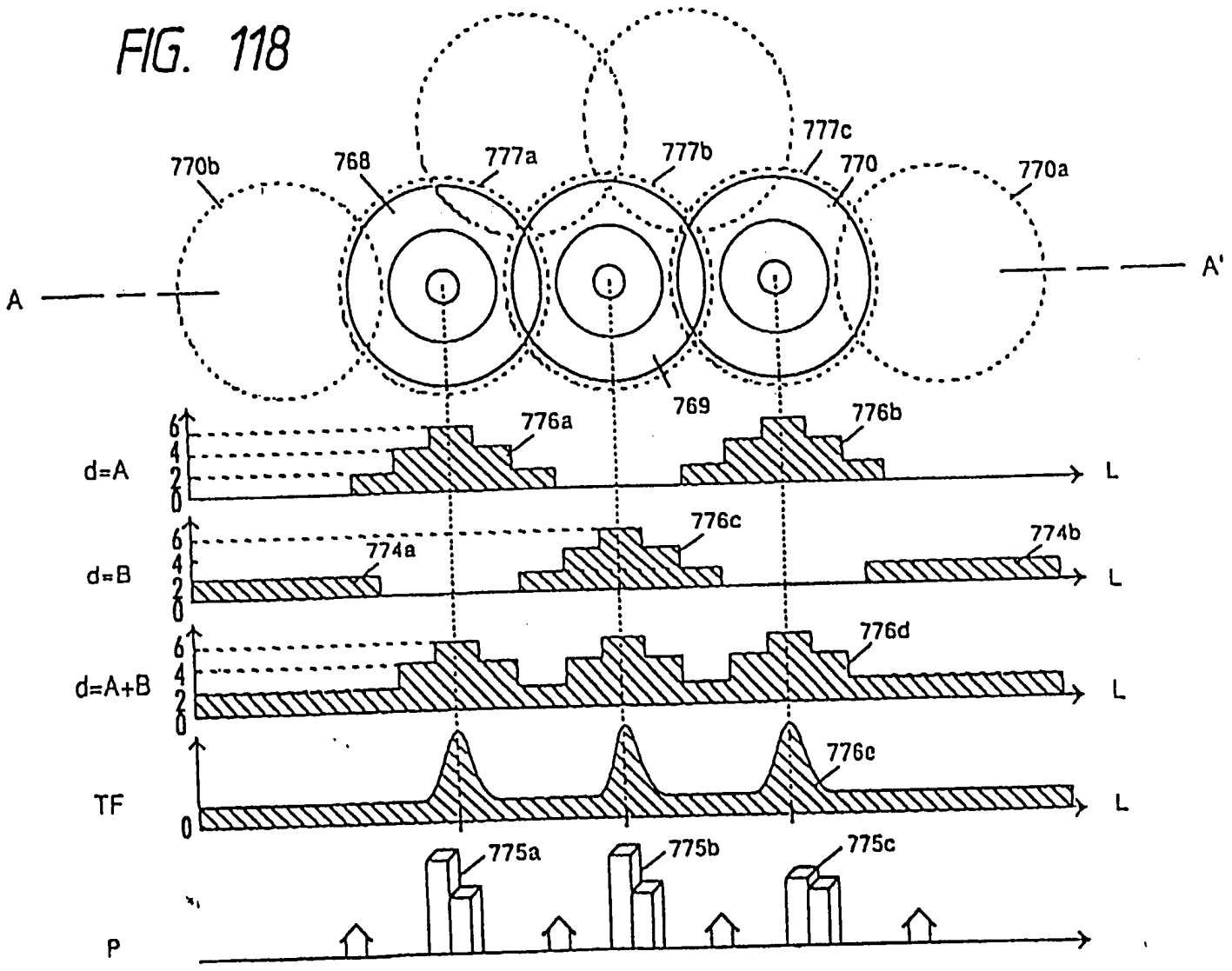

770b
768
777a
777b
777c
770
770a
A
A'
769
776a
776b
d=A
6
4
2
0
L
776c
774a
774b
d=B
776d
d=A+B
776e
TF
775a
775b
775c
P

FIG. 119(a)

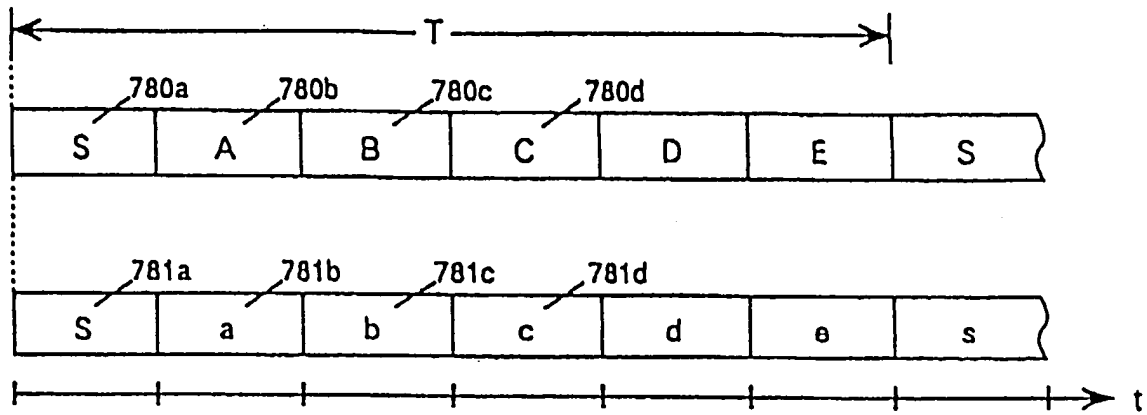


FIG. 119(b)

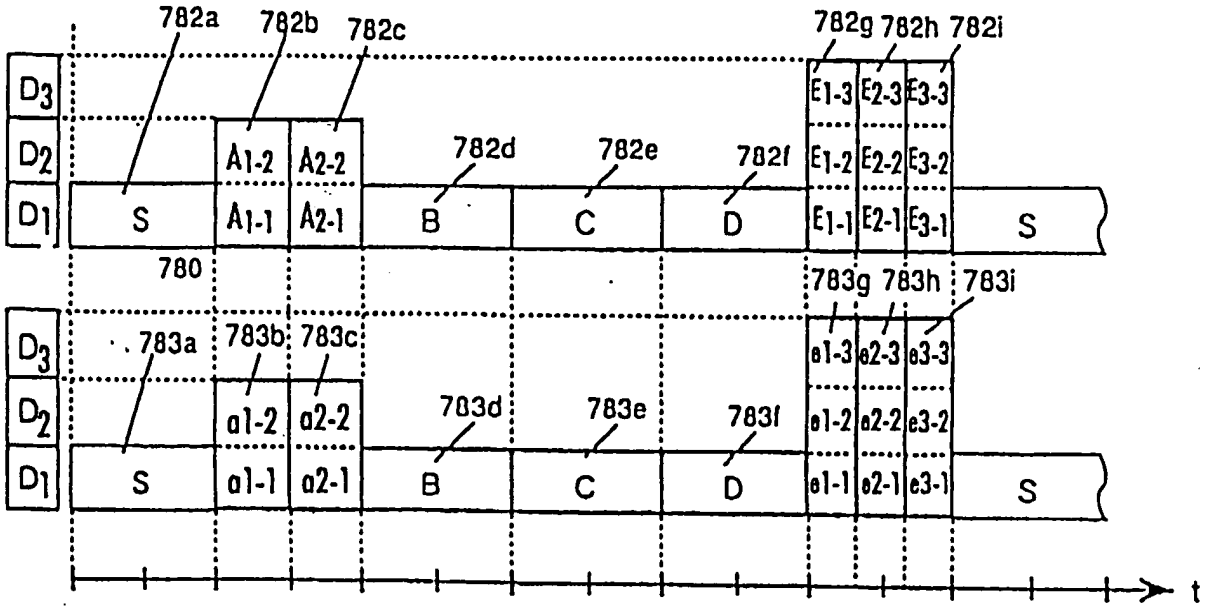


FIG. 120(a)

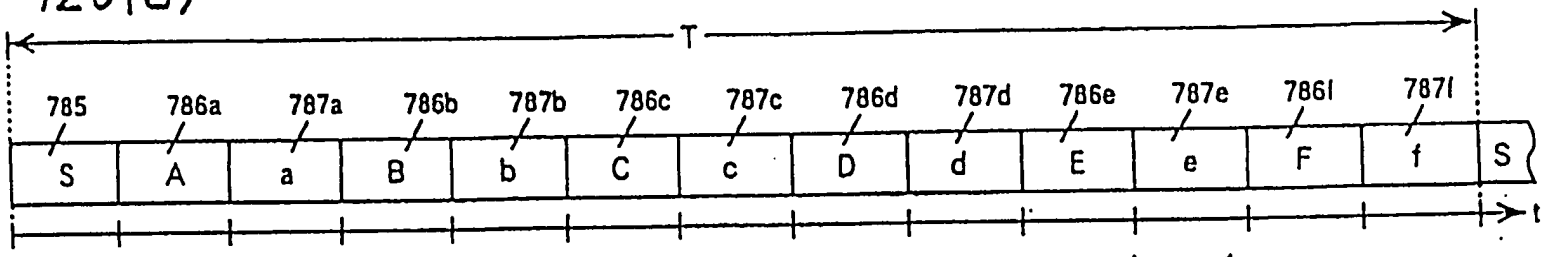


FIG. 120(b)

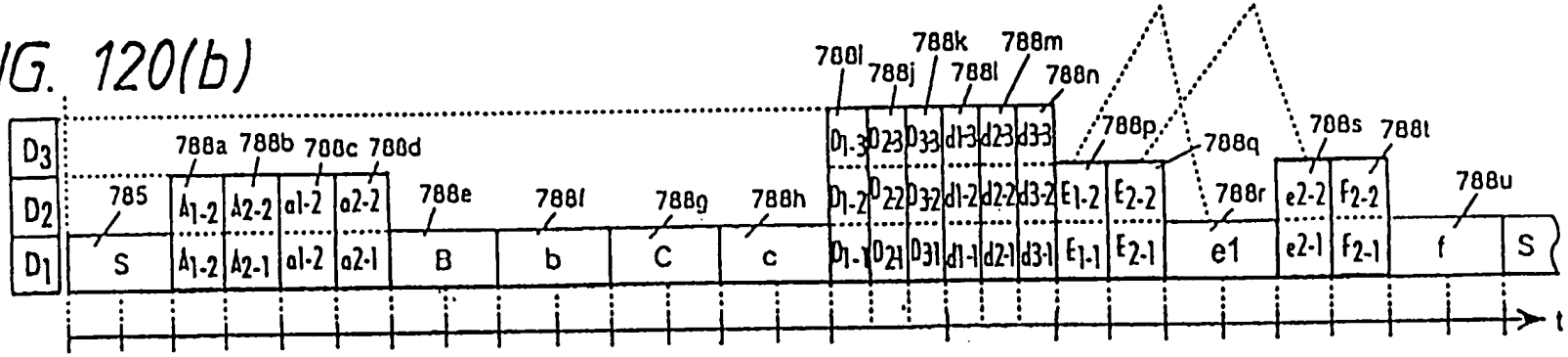


FIG. 121

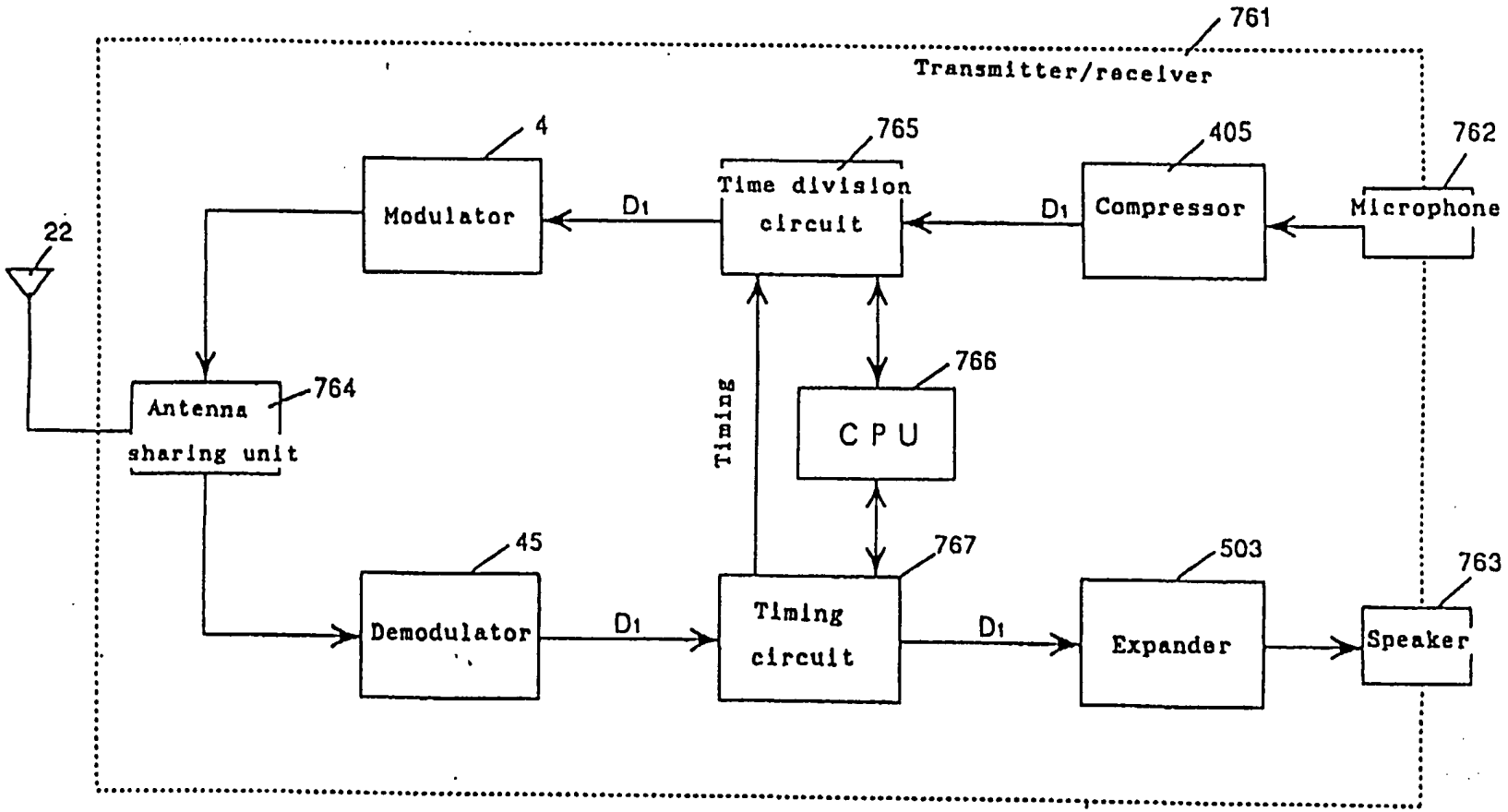

761
Transmitter/receiver
4
Modulator
765
Time division circuit
405
Compressor
762
Microphone
22
D1
D1
764
Antenna sharing unit
766
CPU
Timing
45
Demodulator
767
Timing circuit
503
Expander
763
Speaker
D1
D1

FIG. 122

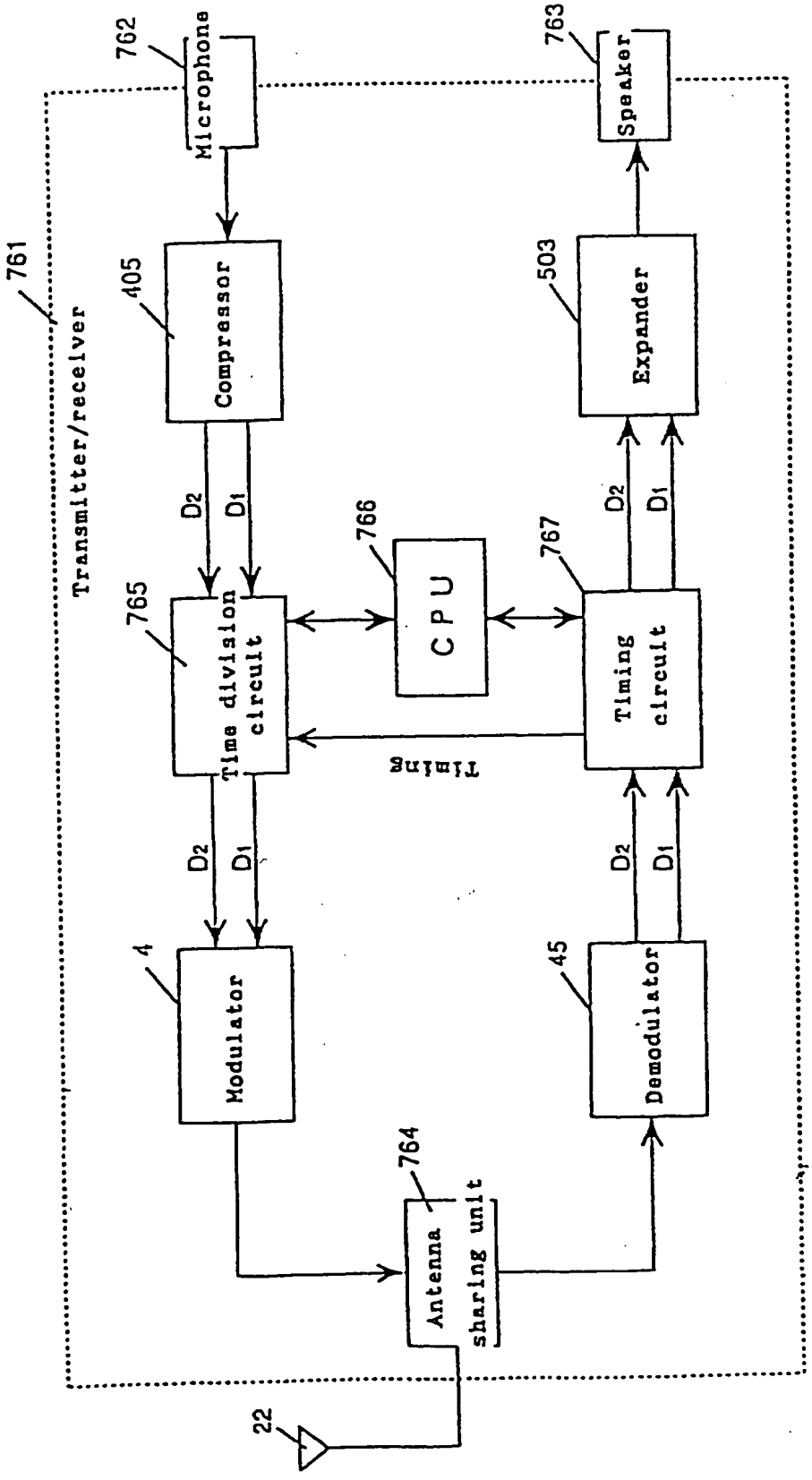

761
Transmitter/receiver
762
Microphone
763
Speaker
405
Compressor
503
Expander
D2
D1
766
CPU
767
765
Time division circuit
Timing circuit
Timing
4
Modulator
45
Demodulator
764
Antenna sharing unit
22

FIG. 123

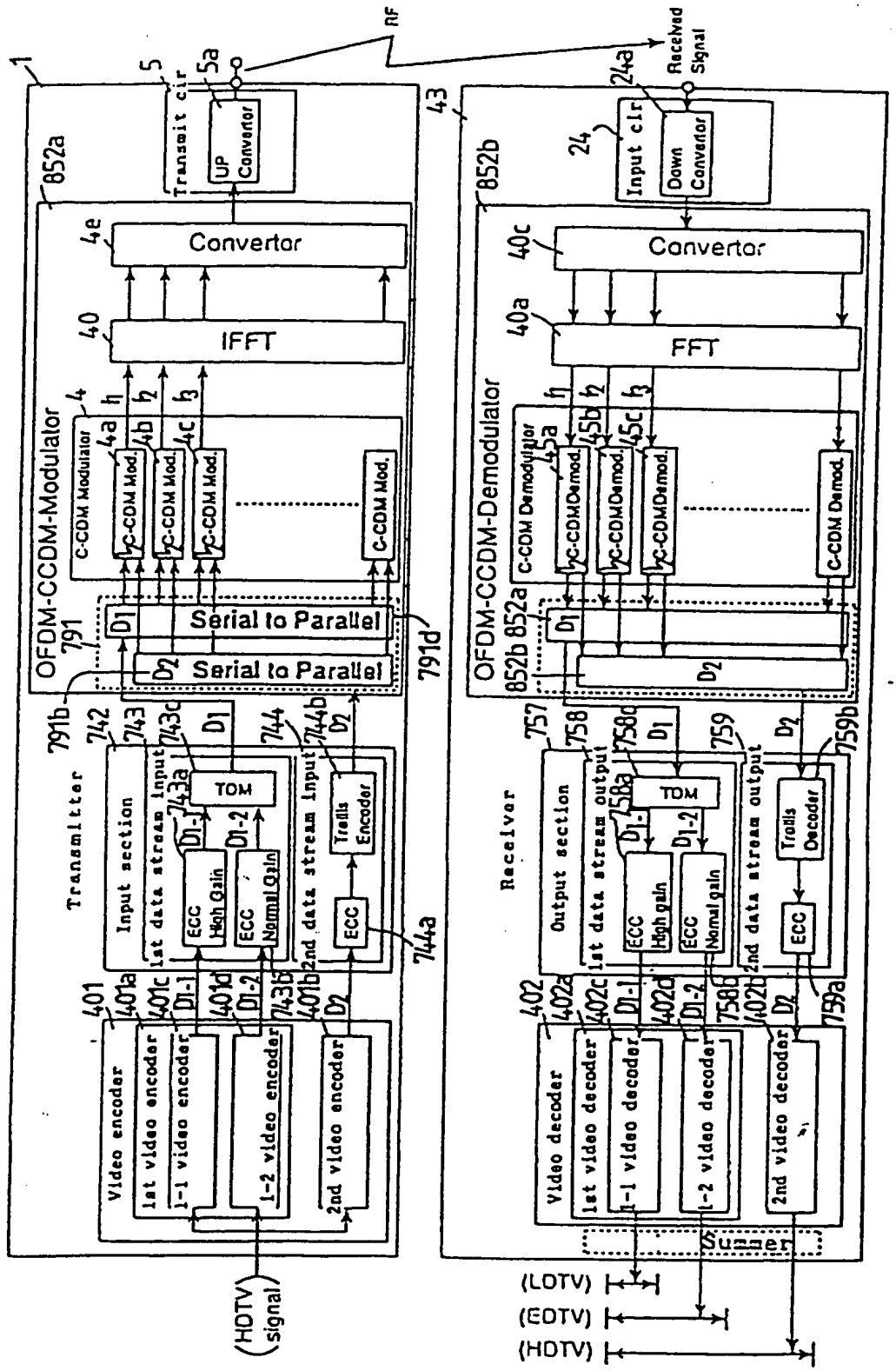

1
5
5a
RF
Transmitter
852a
Transmit clr
UP Convertor
4e
Convertor
40
IFFT
4
OFDM-CCDM-Modulator
C-CDM Modulator
4a
4b
4c
C-CDM Mod.
h1
h2
h3
791
D1
Serial to Parallel
D2
Serial to Parallel
791b
791d
742
743
743c
744
744b
Input section
1st data stream input
2nd data stream input
TDM
D1-1
D1-2
D2
ECC
High Gain
ECC
Normal Gain
Trellis Encoder
ECC
744a
401
401a
401c
401d
401b
Video encoder
1st video encoder
1-1 video encoder
1-2 video encoder
2nd video encoder
(HDTV signal)
43
852b
Receiver
24a
Received Signal
24
Input clr
Down Convertor
40c
Convertor
40a
FFT
OFDM-CCDM-Demodulator
C-CDM Demodulator
45a
45b
45c
C-CDM Demod.
852b 852a
757
758
758c
759
759b
Output section
1st data stream output
2nd data stream output
TDM
D1-1
D1-2
D2
ECC
High gain
ECC
Normal gain
Trellis Decoder
ECC
758a
758b
759a
402
402a
402c
402d
402b
Video decoder
1st video decoder
1-1 video decoder
1-2 video decoder
2nd video decoder
Summer
(LOTV)
(EDTV)
(HDTV)

FIG. 124

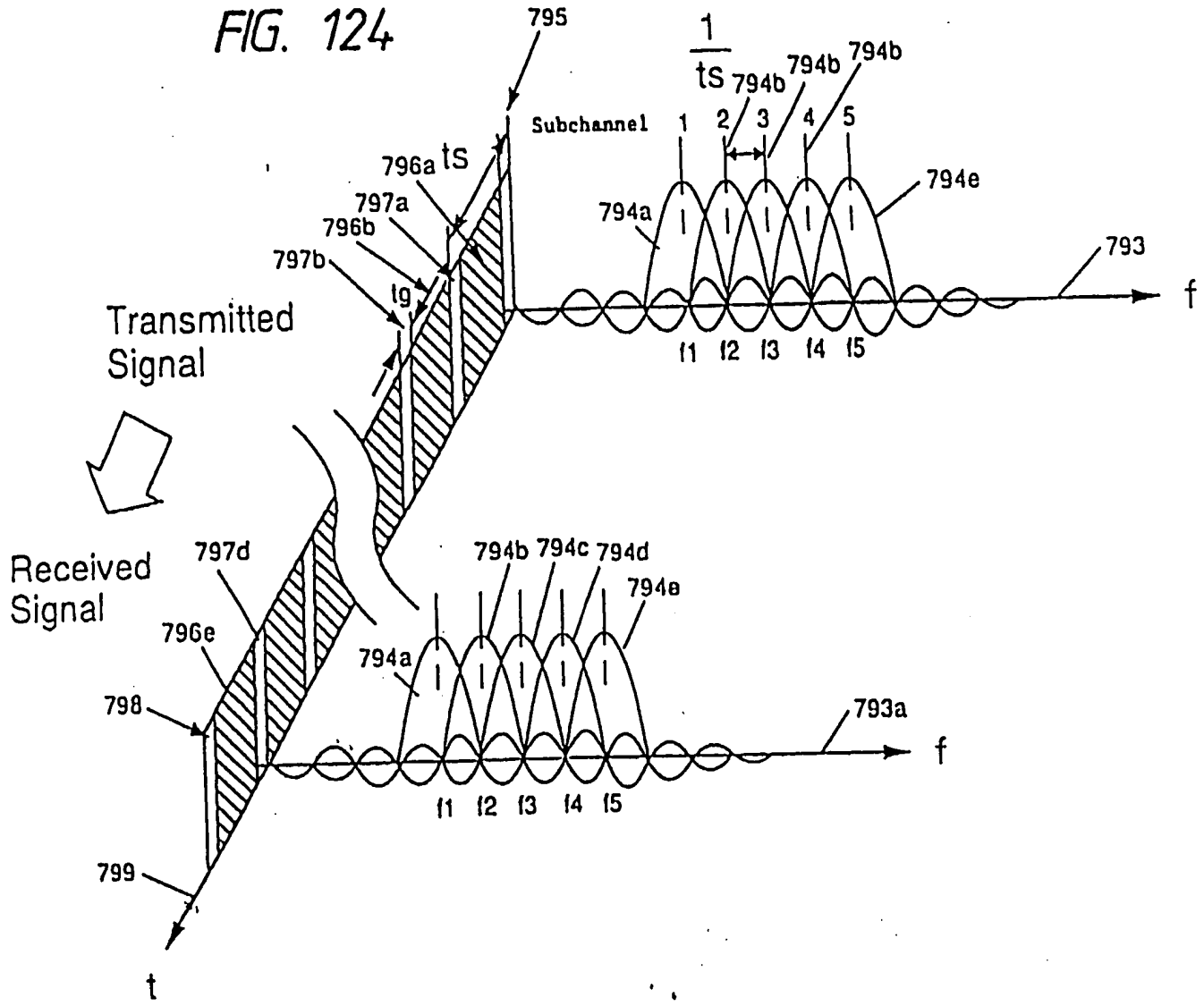

795
1/tS
794b
794b
794b
Subchannel
1
2
3
4
5
796a
tS
797a
796b
797b
tg
794a
794e
793
f
Transmitted Signal
f1 f2 f3 f4 f5
Received Signal
797d
794b
794c
794d
794e
796e
794a
798
793a
f
f1 f2 f3 f4 f5
799
t

FIG. 125(a)

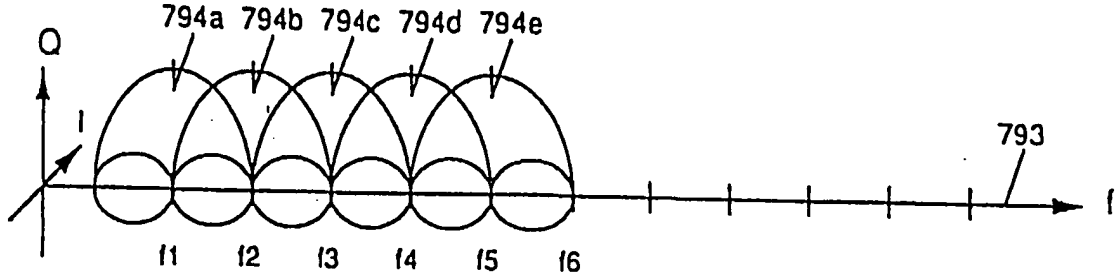
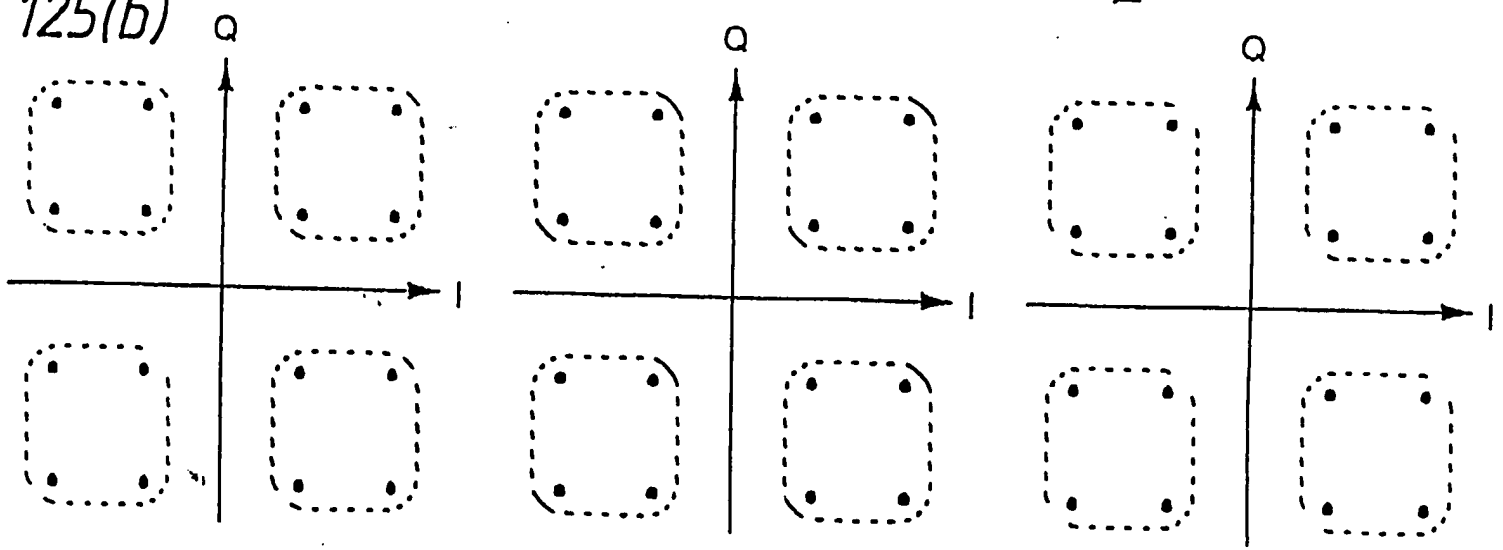


FIG. 125(b)



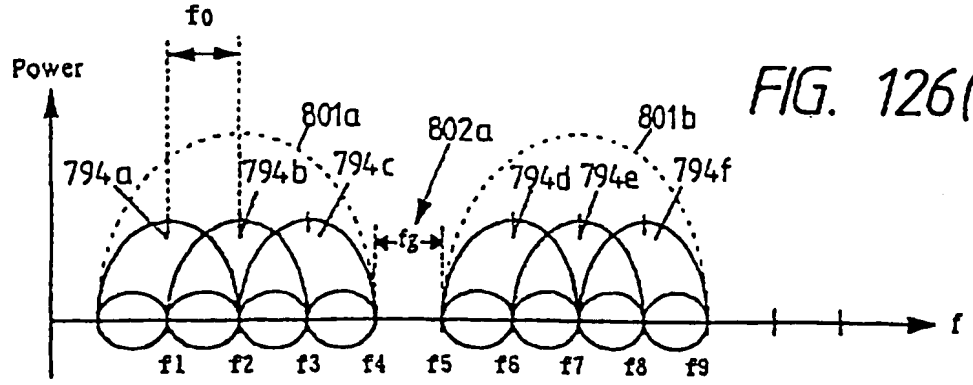


FIG. 126(a)

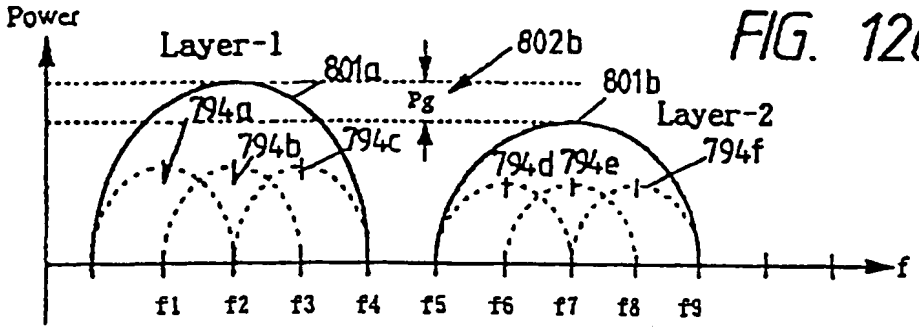


FIG. 126(b)

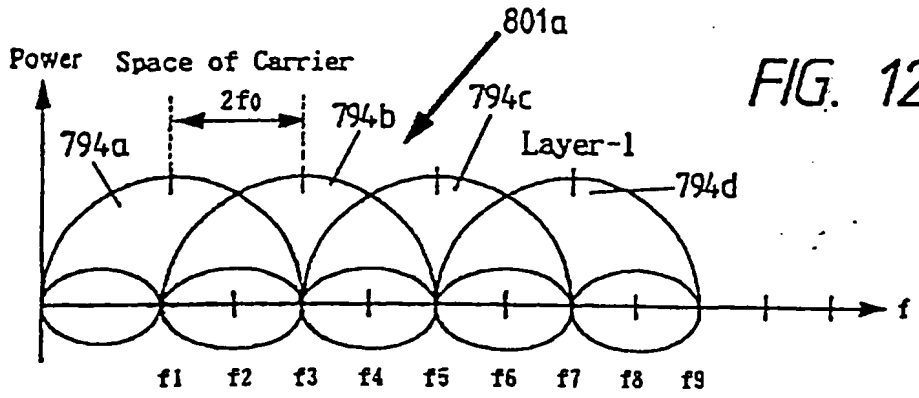


FIG. 126(c)

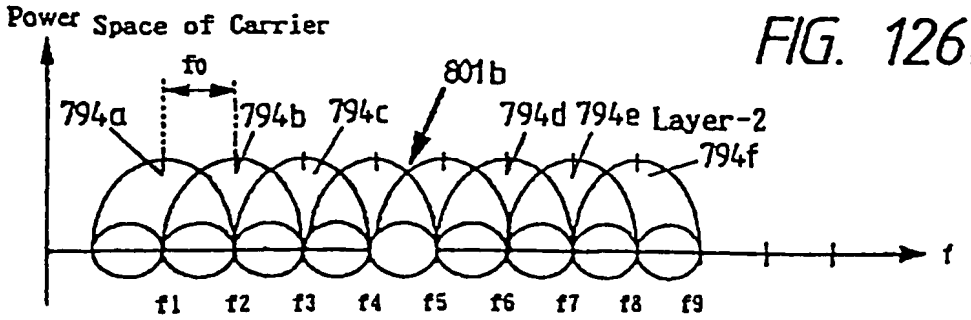


FIG. 126(d)

FIG. 127

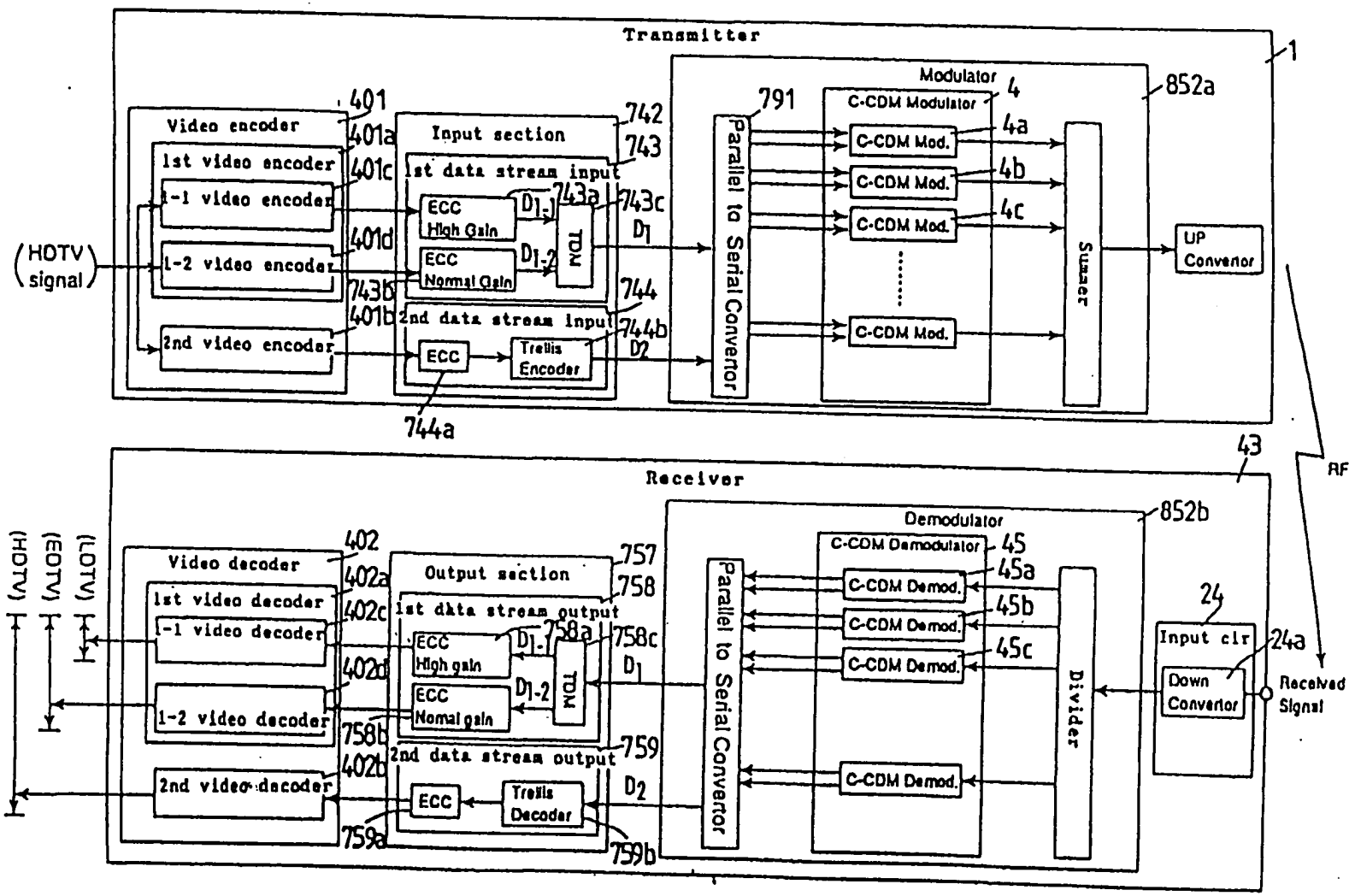

Transmitter
1
Modulator
4
852a
Video encoder
401
1st video encoder
401a
1-1 video encoder
401c
1-2 video encoder
401d
2nd video encoder
401b
(HDTV signal)
Input section
742
1st data stream input
743
ECC High Gain
743a
ECC Normal Gain
743b
TDN
743c
2nd data stream input
744
ECC
744a
Trellis Encoder
744b
D1-1
D1-2
D1
D2
Parallel to Serial Convertor
791
C-CDM Modulator
C-CDM Mod.
4a
4b
4c
Summer
UP Convertor
RF
43
Receiver
852b
Demodulator
C-CDM Demodulator
45
45a
45b
45c
C-CDM Demod.
Divider
24
Input clr
24a
Down Convertor
Received Signal
Video decoder
402
1st video decoder
402a
1-1 video decoder
402c
1-2 video decoder
402d
2nd video decoder
402b
(HDTV)
(EDTV)
(LDTV)
Output section
757
1st data stream output
758
ECC High gain
758a
ECC Nomal gain
758b
TDN
758c
2nd data stream output
759
ECC
759a
Trellis Decoder
759b
D1-1
D1-2
D1
D2
Parallel to Serial Convertor

FIG. 128(a)

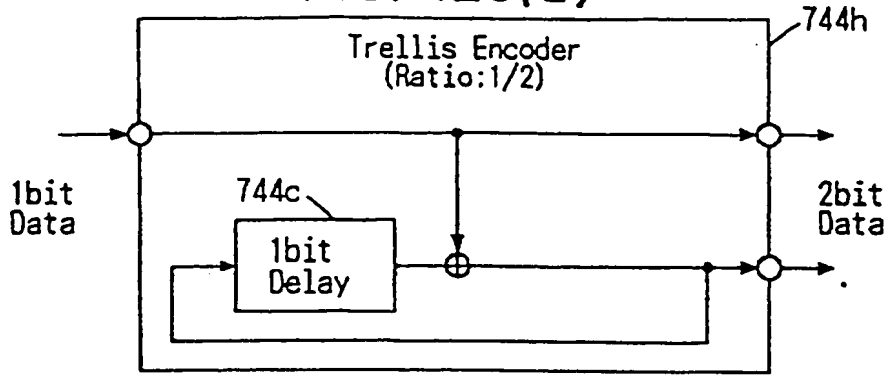


FIG. 128(b)

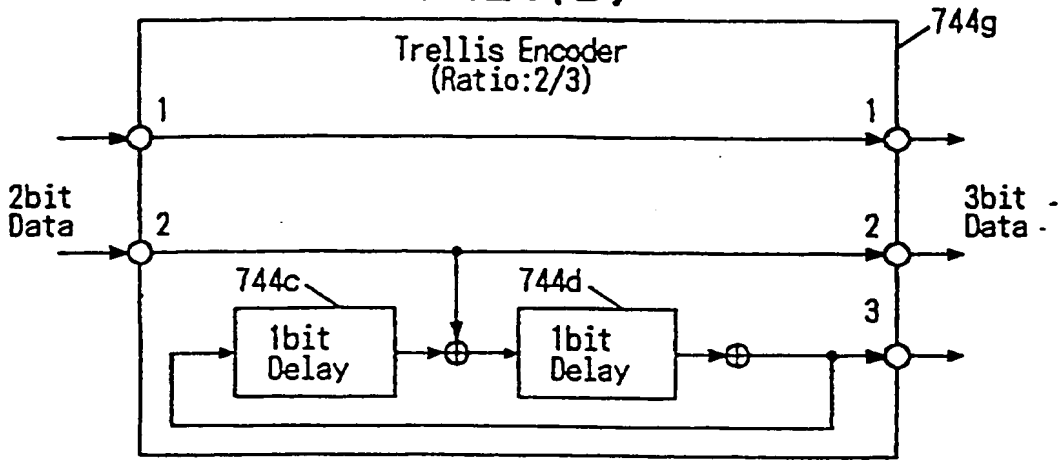


FIG. 128(c)

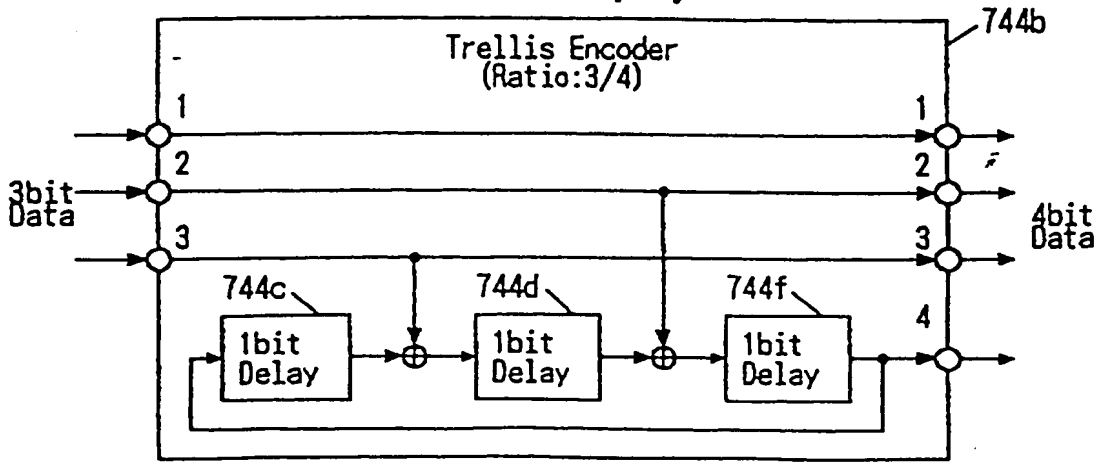


FIG. 128(d)

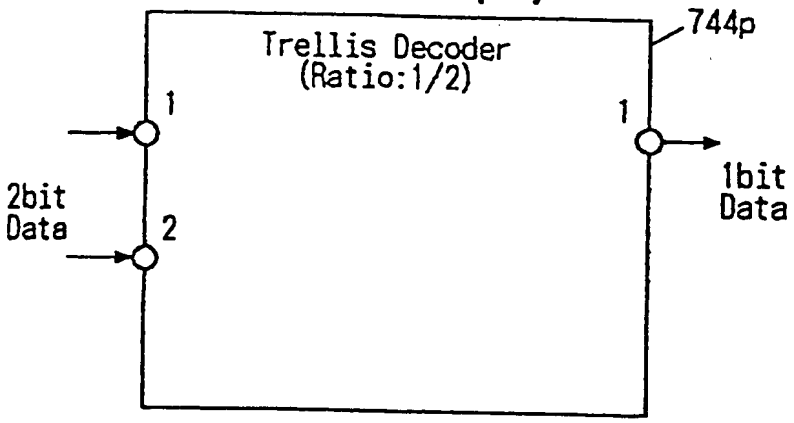


FIG. 128(e)

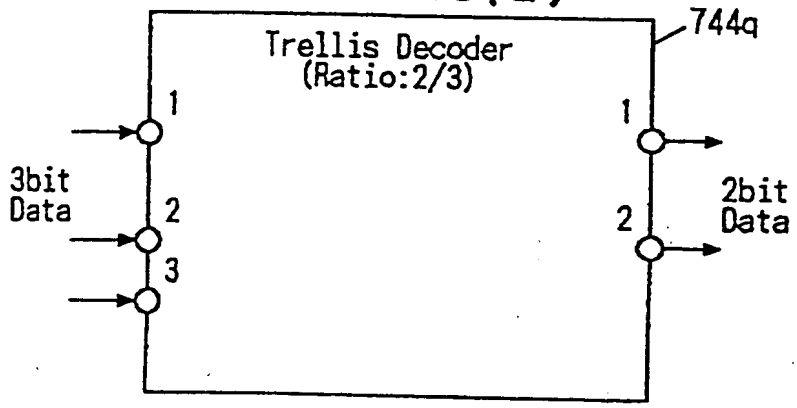


FIG. 128(f)

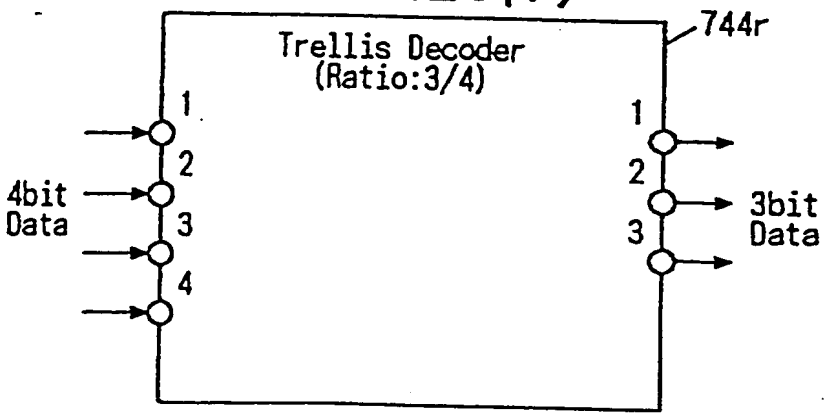


FIG. 129

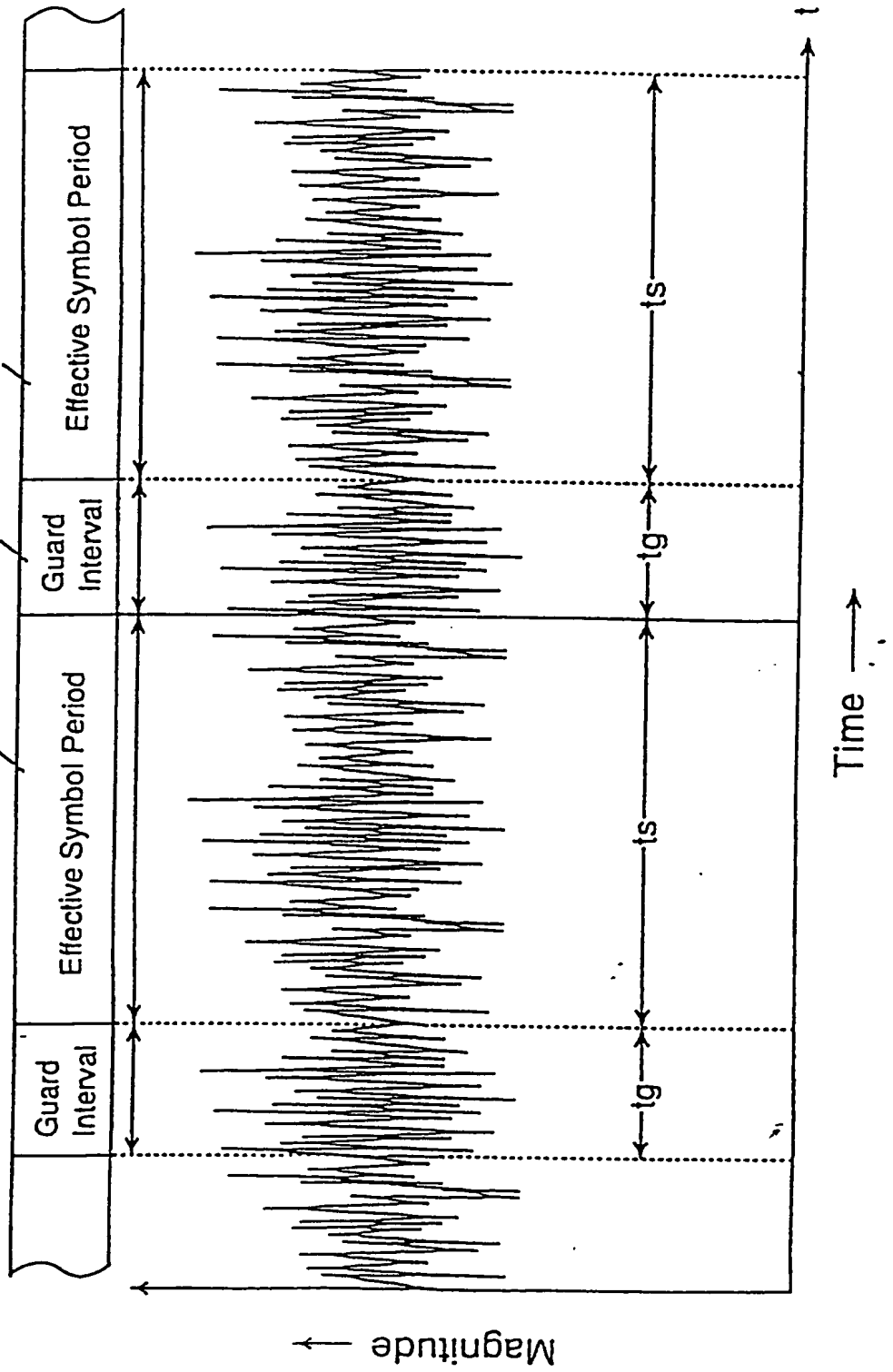
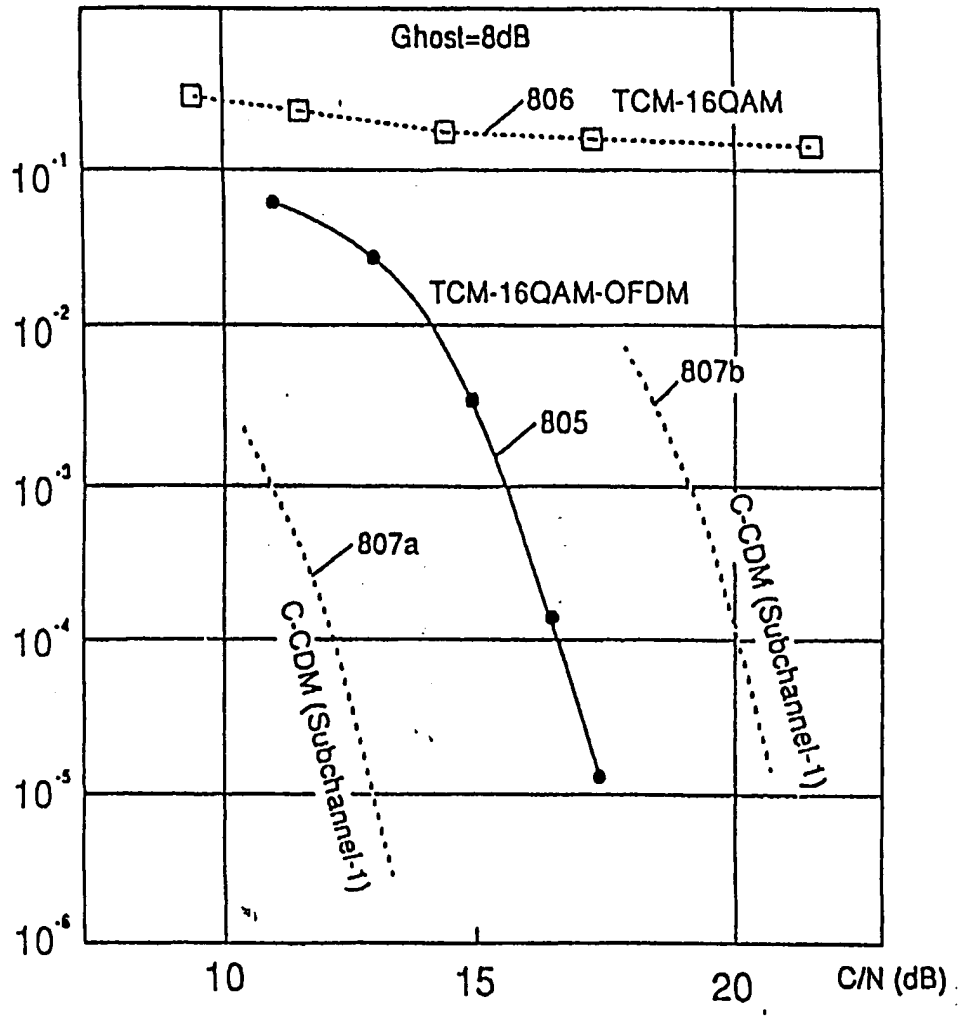

Guard Interval
Effective Symbol Period
Guard Interval
Effective Symbol Period
796a
797a
796b
tg
ts
tg
ts
Time
Magnitude
t

FIG. 130



GHOST DELAY=2us, D/U=8dB

Figure 8 Bit Error Rate Performance Under Single Ghost and Gaussian Noise (1)

FIG. 131

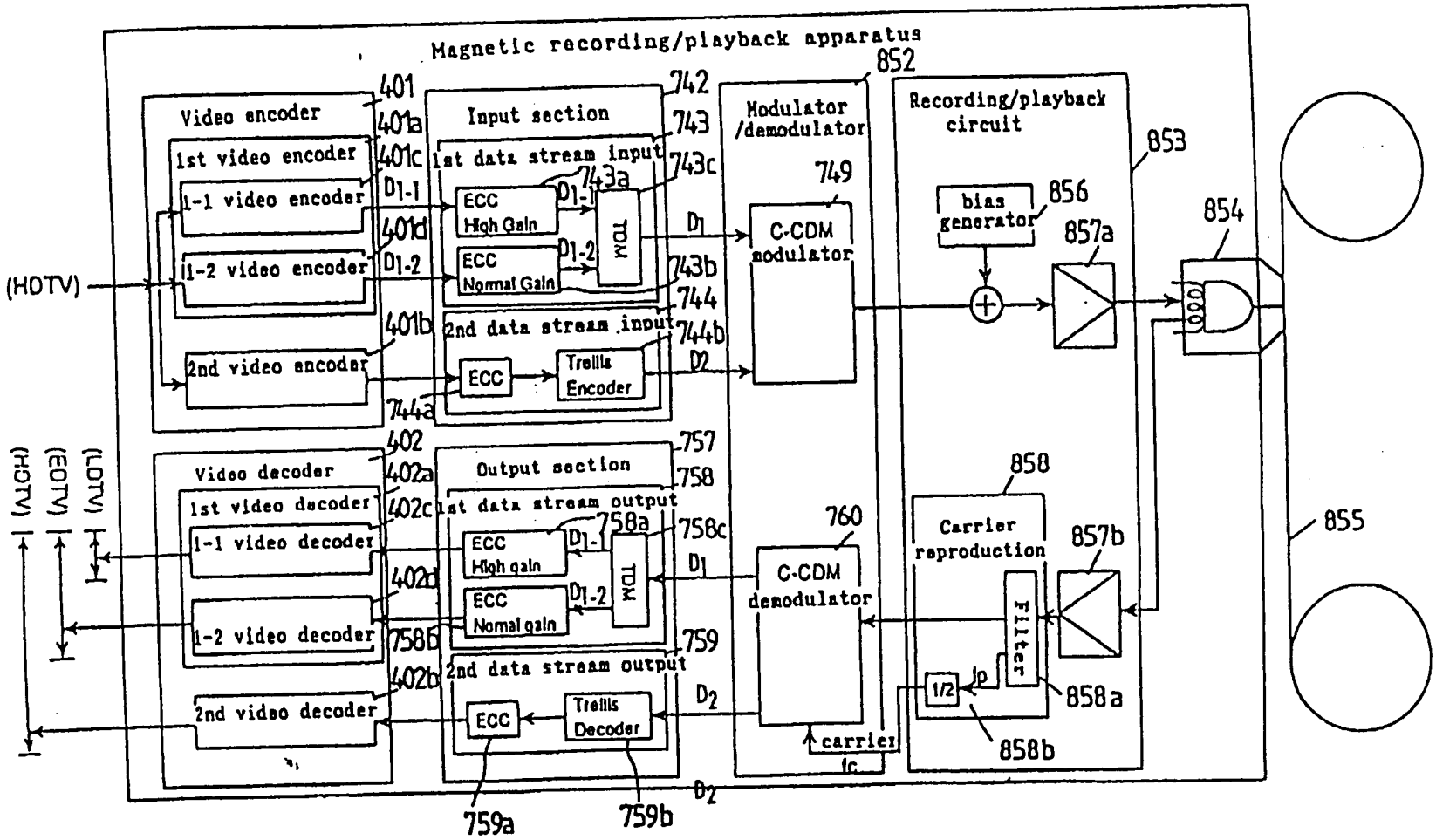

Magnetic recording/playback apparatus
Video encoder
401
401a
1st video encoder
401c
1-1 video encoder
D1-1
401d
1-2 video encoder
D1-2
401b
2nd video encoder
Input section
742
743
1st data stream input
743c
743a
ECC
High Gain
D1-1
TDM
D1
ECC
Normal Gain
D1-2
743b
744
2nd data stream input
744b
ECC
Trellis
Encoder
D2
744a
Modulator
/demodulator
852
749
C-CDM
modulator
Recording/playback
circuit
853
bias
generator
856
857a
854
(HDTV)
Video decoder
402
402a
1st video decoder
402c
1-1 video decoder
402d
1-2 video decoder
758b
402b
2nd video decoder
Output section
757
758
1st data stream output
758a
758c
ECC
High gain
D1-1
TDM
D1
ECC
Normal gain
D1-2
759
2nd data stream output
ECC
Trellis
Decoder
D2
759a
759b
760
C-CDM
demodulator
carrier
fc
858
Carrier
reproduction
857b
Filter
1/2
fp
858a
858b
855
(HDTV)
(EDTV)
(LDTV)
D2

FIG. 132

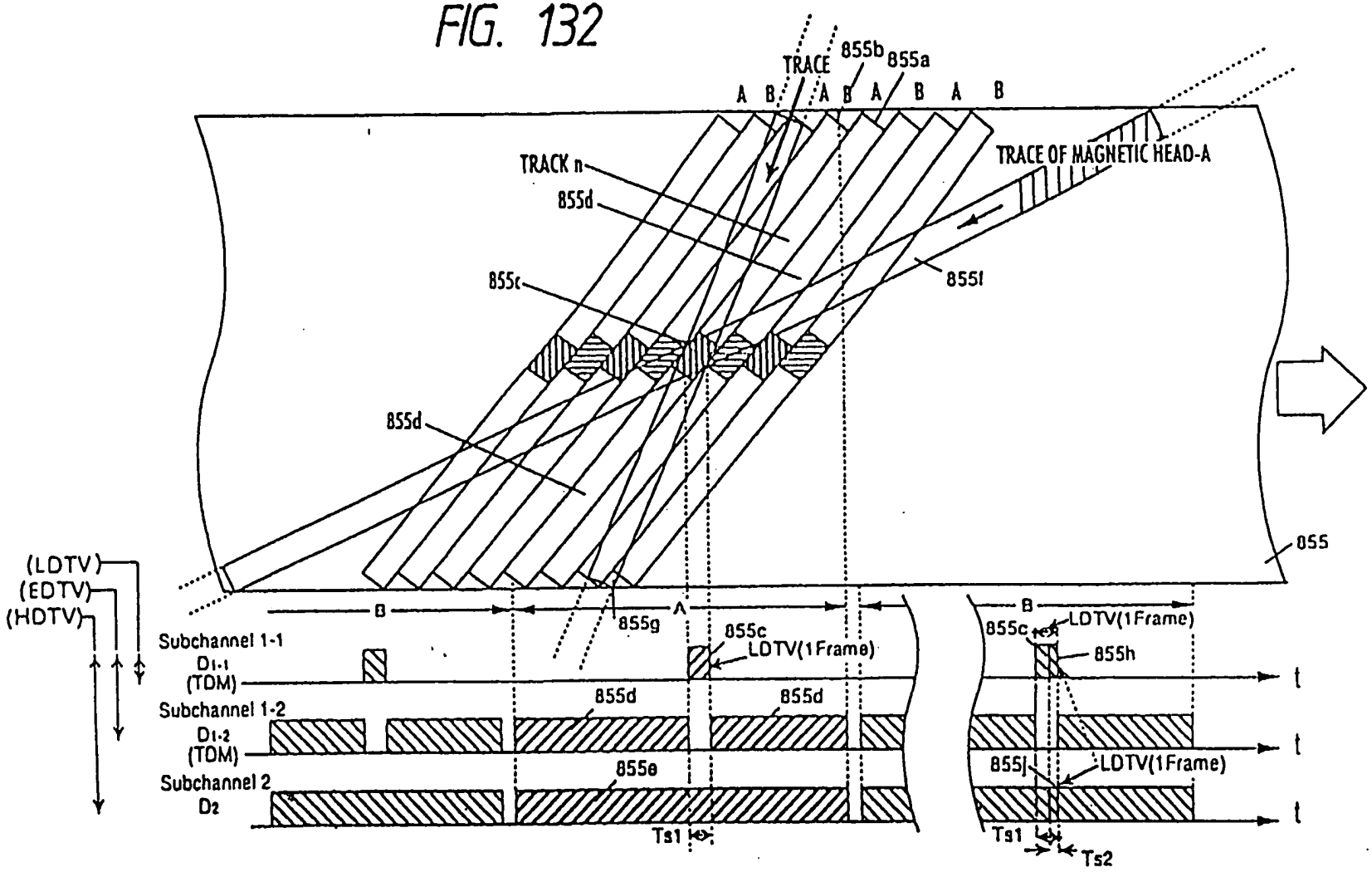

TRACE
855b
855a
A B A B A B A B
TRACK n
855d
855c
TRACE OF MAGNETIC HEAD-A
855f
855d
855
(LDTV)
(EDTV)
(HDTV)
B
A
855g
855c
LDTV(1Frame)
Subchannel 1-1
D1-1
(TDM)
Subchannel 1-2
D1-2
(TDM)
855d
855d
Subchannel 2
D2
855e
Ts1
B
855c
LDTV(1Frame)
855h
855j
LDTV(1Frame)
Ts1
Ts2
t
t
t

FIG. 133

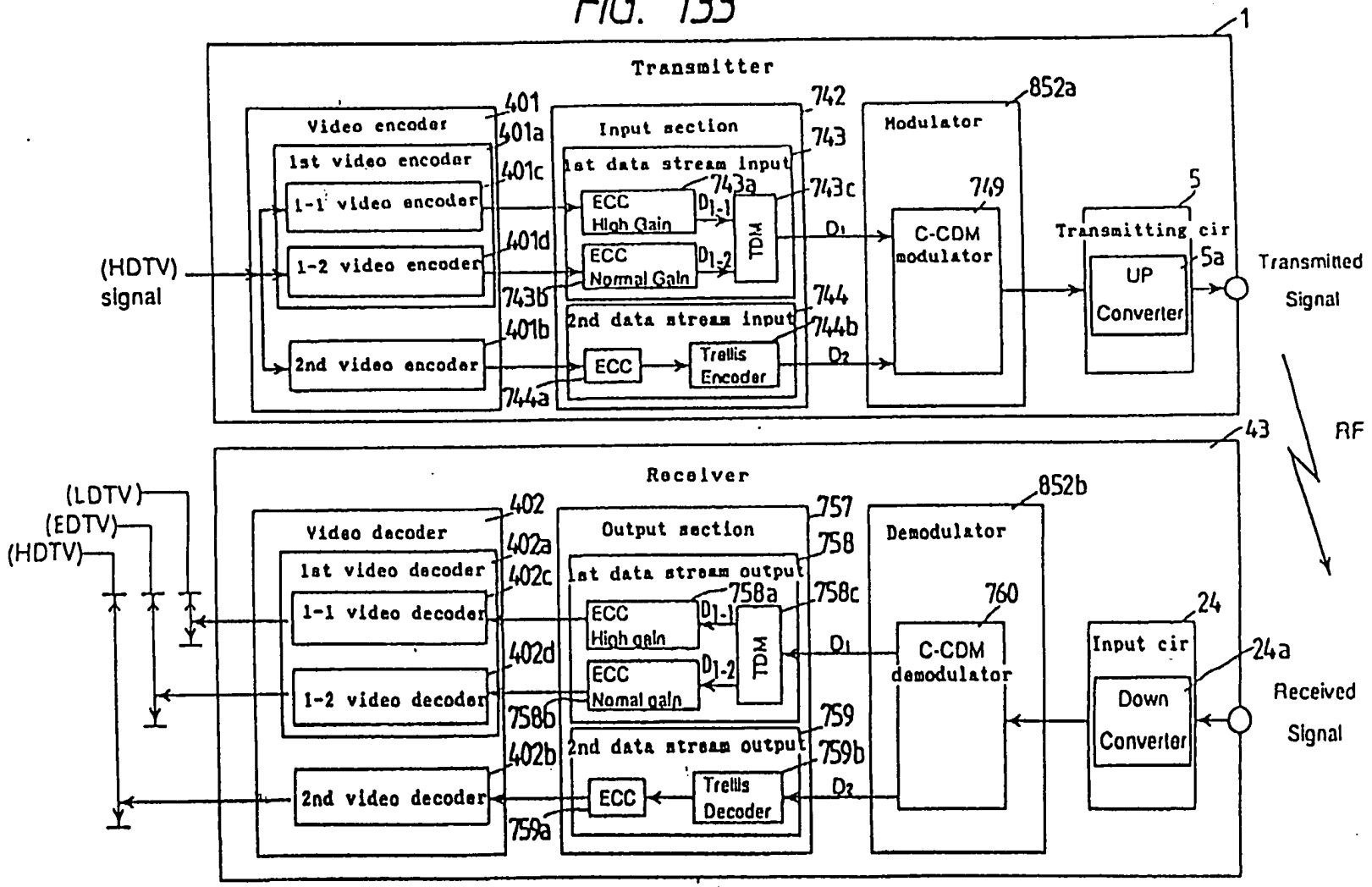

1
Transmitter
401
Video encoder
401a
1st video encoder
401c
1-1 video encoder
401d
1-2 video encoder
401b
2nd video encoder
(HDTV) signal
742
Input section
743
1st data stream input
743a
ECC High Gain
D1-1
TDM
743c
D1
743b
ECC Normal Gain
D1-2
744
2nd data stream input
744b
ECC
Trellis Encoder
D2
744a
852a
Modulator
749
C-CDM modulator
5
Transmitting cir
5a
UP Converter
Transmitted Signal
RF
43
Receiver
(LDTV)
(EDTV)
(HDTV)
402
Video decoder
402a
1st video decoder
402c
1-1 video decoder
402d
1-2 video decoder
402b
2nd video decoder
757
Output section
758
1st data stream output
758a
ECC High gain
D1-1
TDM
758c
D1
758b
ECC Nomal gain
D1-2
759
2nd data stream output
759b
ECC
Trellis Decoder
D2
759a
852b
Demodulator
760
C-CDM demodulator
24
Input cir
24a
Down Converter
Received Signal

FIG. 134

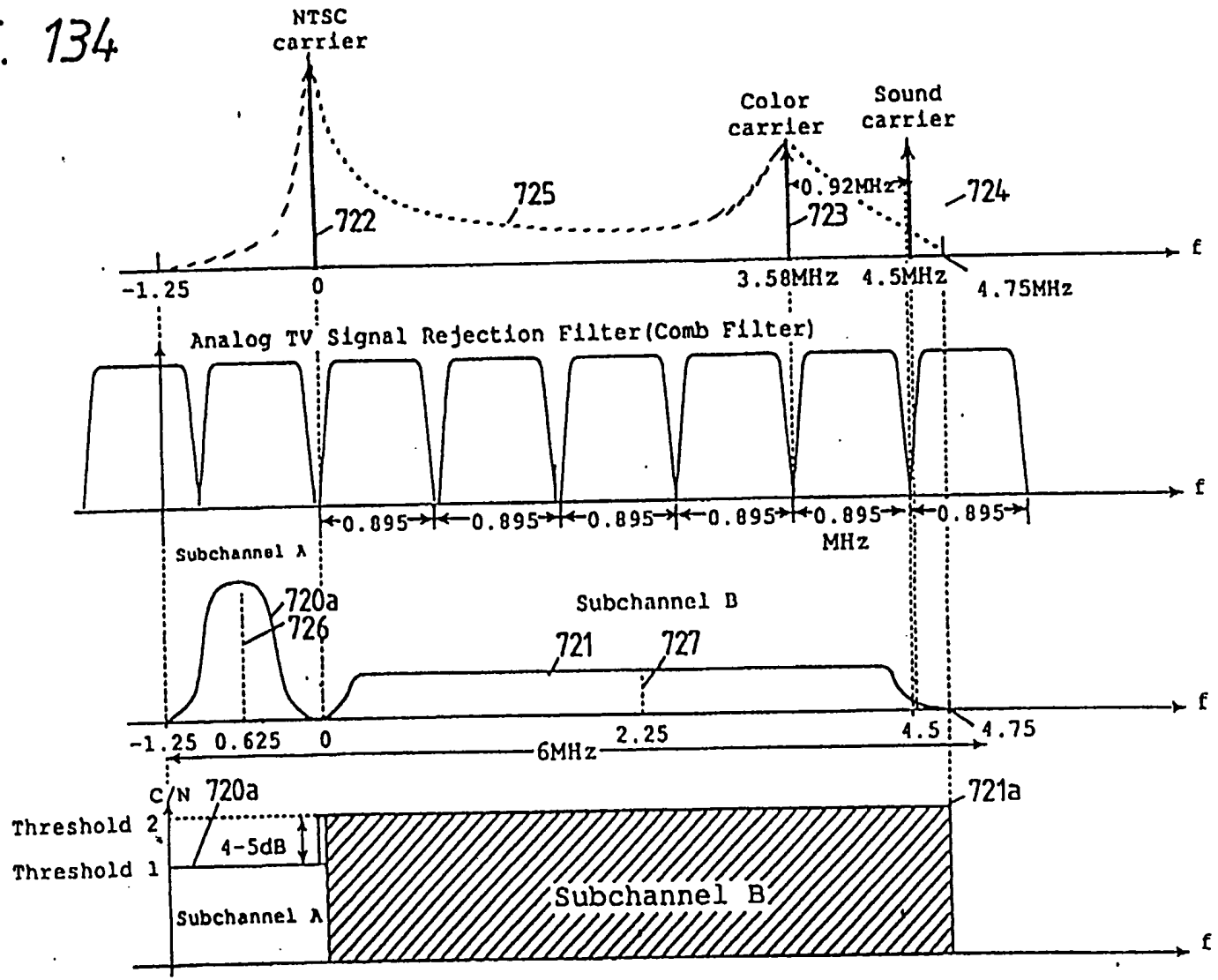

NTSC carrier
Color carrier
Sound carrier
0.92MHz
722
725
723
724
f
-1.25
0
3.58MHz
4.5MHz
4.75MHz
Analog TV Signal Rejection Filter(Comb Filter)
0.895
0.895
0.895
0.895
0.895
0.895
MHz
Subchannel A
720a
726
Subchannel B
721
727
-1.25
0.625
0
2.25
4.5
4.75
6MHz
C/N
720a
721a
Threshold 2
Threshold 1
4-5dB
Subchannel A
Subchannel B

FIG. 135

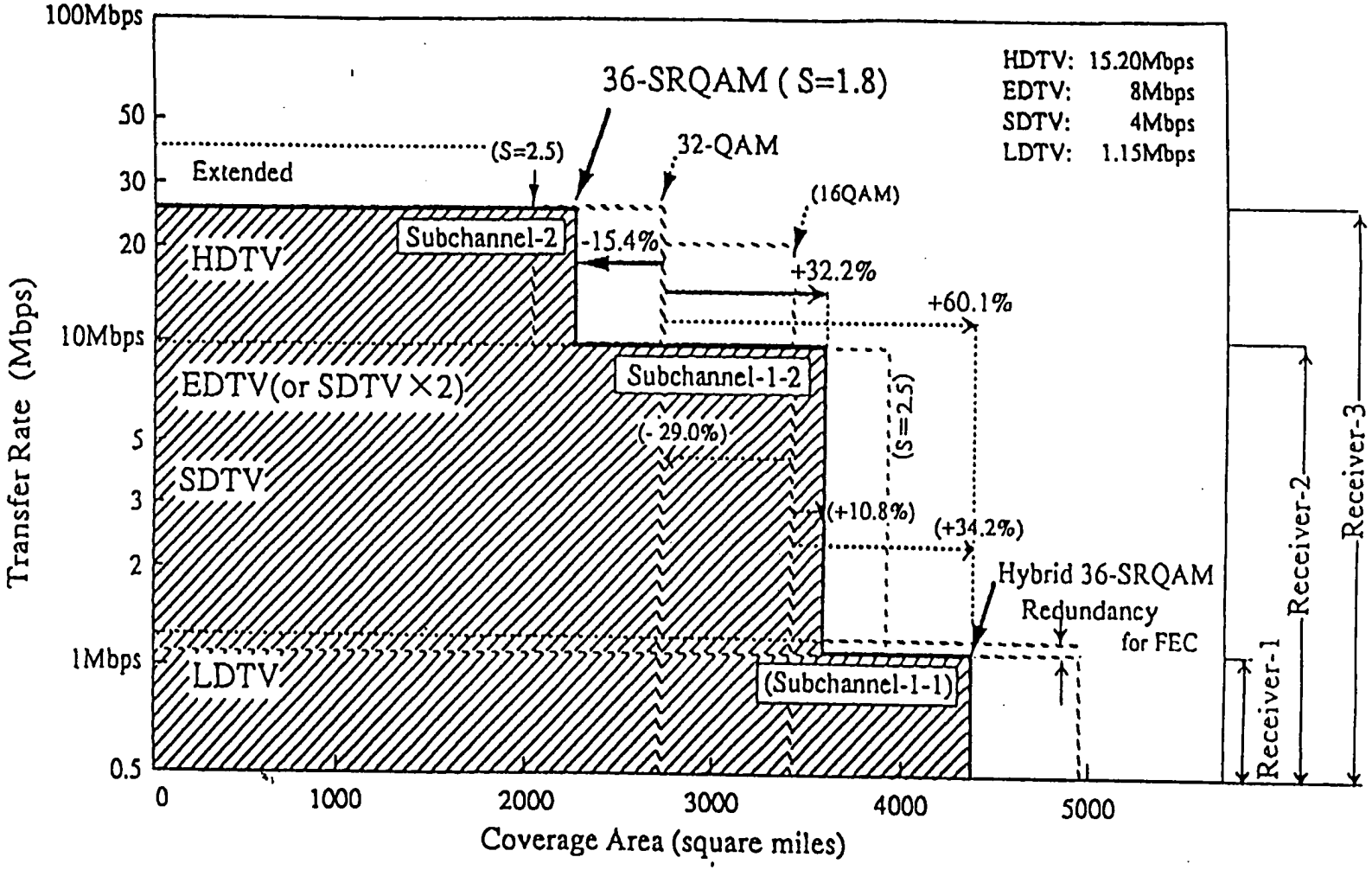

100Mbps
50
30
20
10Mbps
5
3
2
1Mbps
0.5
Transfer Rate (Mbps)
0
1000
2000
3000
4000
5000
Coverage Area (square miles)
36-SRQAM (S=1.8)
32-QAM
(16QAM)
(S=2.5)
Extended
HDTV
Subchannel-2
-15.4%
+32.2%
+60.1%
EDTV(or SDTV×2)
Subchannel-1-2
(- 29.0%)
(S=2.5)
SDTV
(+10.8%)
(+34.2%)
Hybrid 36-SRQAM
Redundancy
for FEC
LDTV
(Subchannel-1-1)
HDTV: 15.20Mbps
EDTV: 8Mbps
SDTV: 4Mbps
LDTV: 1.15Mbps
Receiver-1
Receiver-2
Receiver-3

FIG. 136

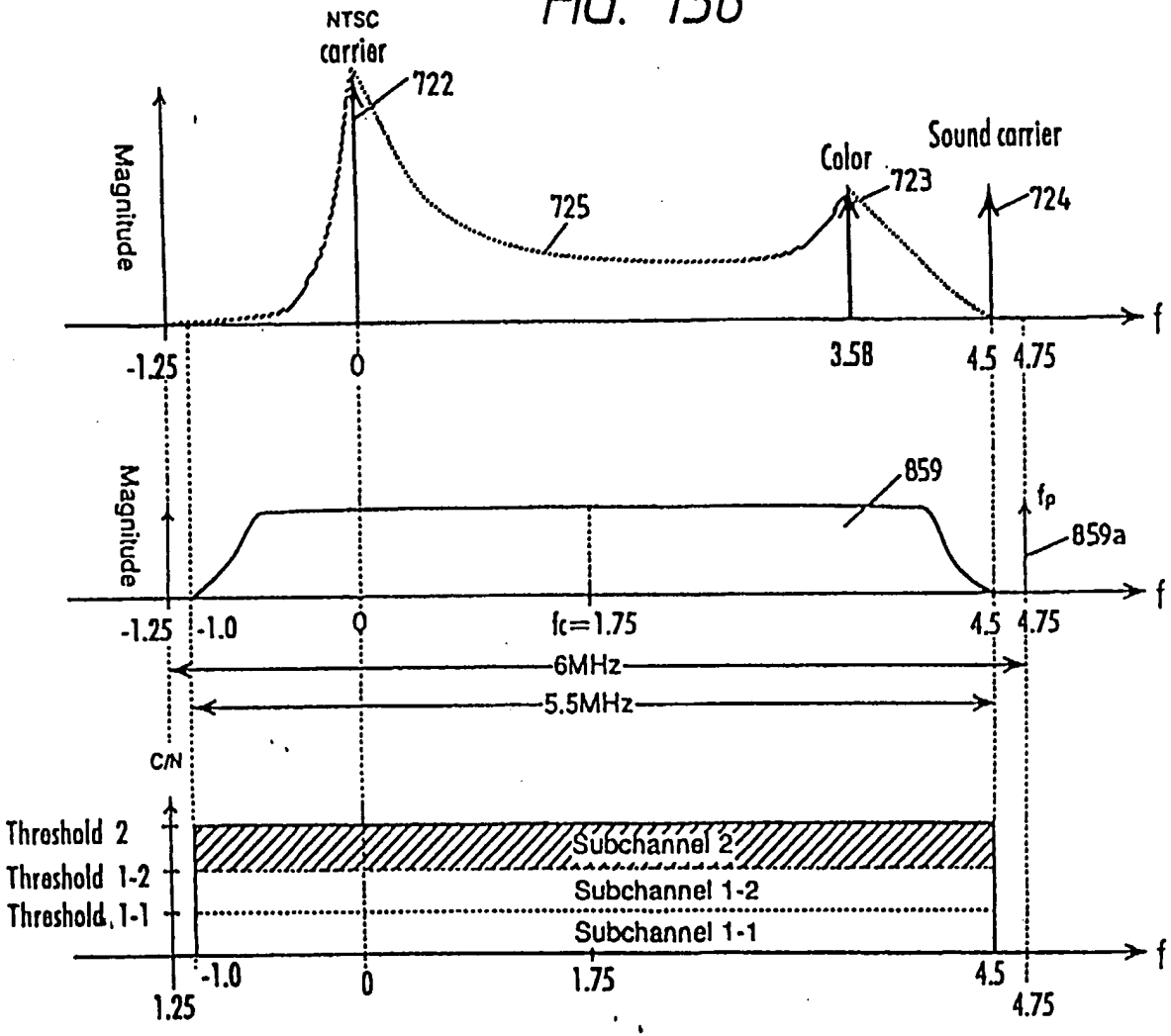

NTSC carrier
722
Color
723
Sound carrier
724
725
Magnitude
f
-1.25
0
3.58
4.5
4.75
859
f_p
859a
-1.0
f_c=1.75
6MHz
5.5MHz
C/N
Threshold 2
Threshold 1-2
Threshold 1-1
Subchannel 2
Subchannel 1-2
Subchannel 1-1
1.25
1.75

FIG. 137

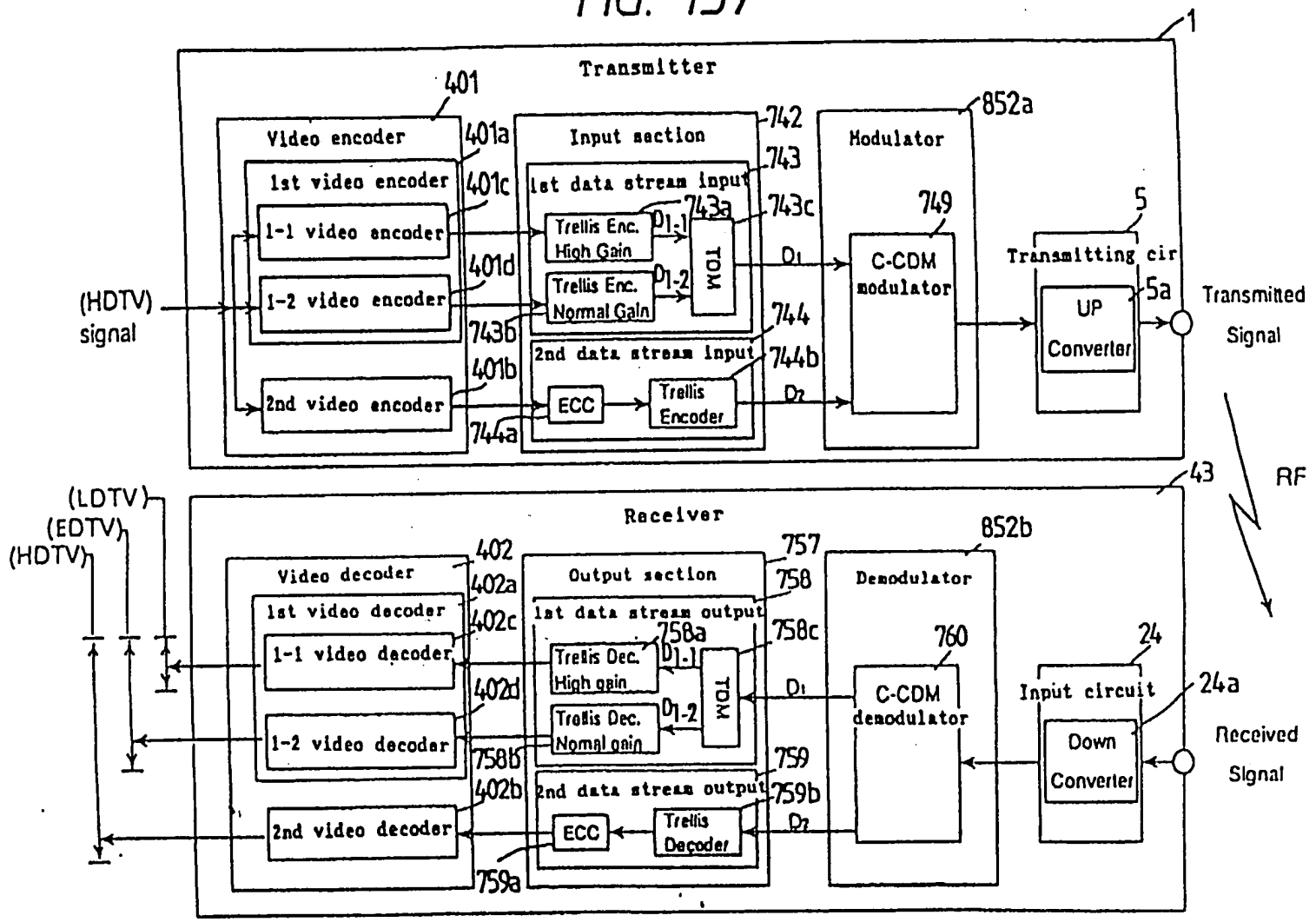

1
Transmitter
401
Video encoder
401a
1st video encoder
401c
1-1 video encoder
401d
1-2 video encoder
401b
2nd video encoder
(HDTV) signal
742
Input section
743
1st data stream input
743a
Trellis Enc. High Gain
D1-1
743c
TDM
Trellis Enc. Normal Gain
D1-2
743b
744
2nd data stream input
744b
ECC
Trellis Encoder
744a
D1
D2
852a
Modulator
749
C-CDM modulator
5
Transmitting cir
5a
UP Converter
Transmitted Signal
RF
43
Receiver
(LDTV)
(EDTV)
(HDTV)
402
Video decoder
402a
1st video decoder
402c
1-1 video decoder
402d
1-2 video decoder
402b
2nd video decoder
757
Output section
758
1st data stream output
758a
Trellis Dec. High gain
D1-1
758c
TDM
Trellis Dec. Nomal gain
D1-2
758b
759
2nd data stream output
759b
ECC
Trellis Decoder
759a
D1
D2
852b
Demodulator
760
C-CDM demodulator
24
Input circuit
24a
Down Converter
Received Signal

FIG. 138

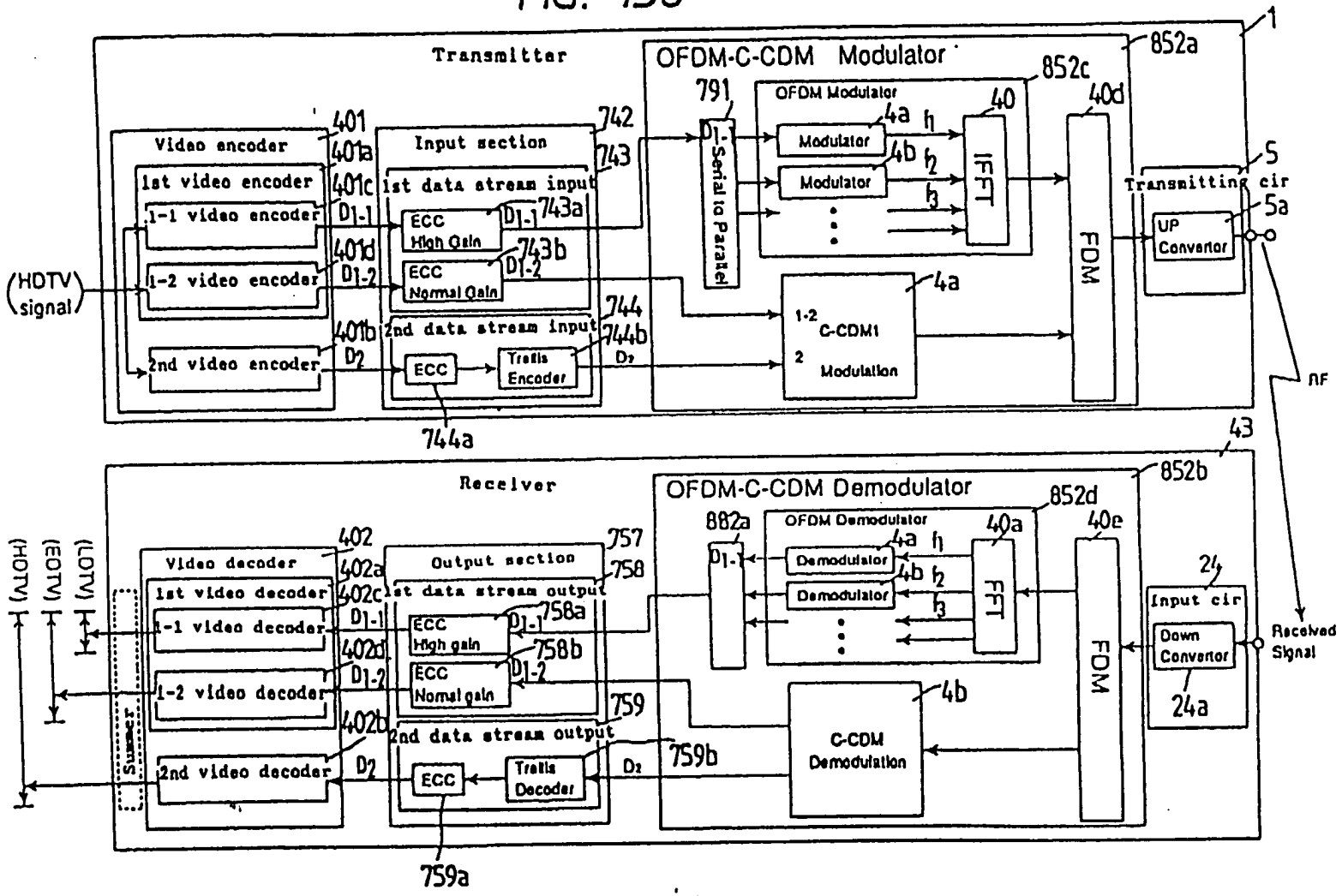

Transmitter
OFDM-C-CDM Modulator
Video encoder
1st video encoder
1-1 video encoder
1-2 video encoder
2nd video encoder
Input section
1st data stream input
ECC High Gain
ECC Normal Gain
2nd data stream input
ECC
Trellis Encoder
Parallel to Serial
OFDM Modulator
Modulator
Modulator
IFFT
C-CDM Modulation
FDM
Transmitting cir
UP Convertor
(HDTV) signal
NF
Receiver
OFDM-C-CDM Demodulator
Video decoder
1st video decoder
1-1 video decoder
1-2 video decoder
2nd video decoder
Output section
1st data stream output
ECC High gain
ECC Normal gain
2nd data stream output
ECC
Trellis Decoder
Serial to Parallel
OFDM Demodulator
Demodulator
Demodulator
FFT
C-CDM Demodulation
FDM
Input cir
Down Convertor
Received Signal
Summer
(HDTV)
(EDTV)
(LDTV)

FIG. 139

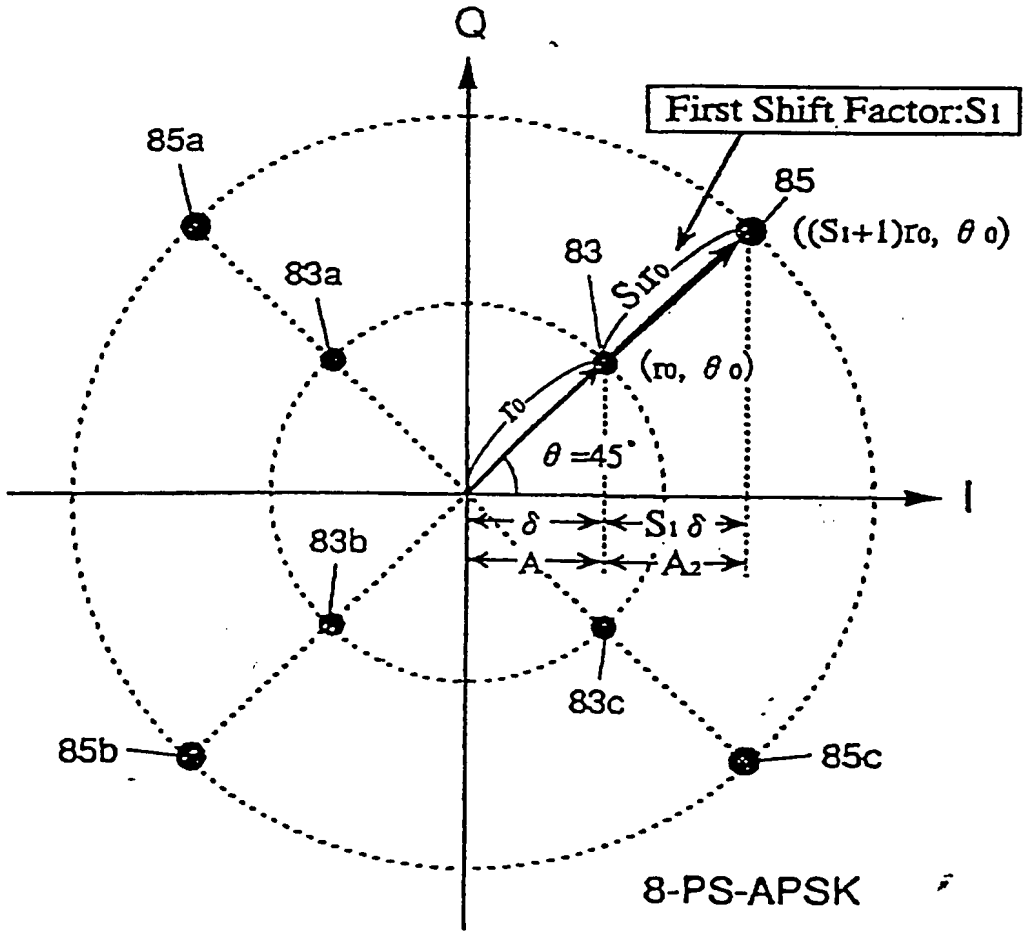

Q
I
First Shift Factor:S1
85a
85
((S1+1)r0, θ 0)
83
S1r0
83a
(r0, θ 0)
r0
θ =45°
δ
S1 δ
A
A2
83b
83c
85b
85c
8-PS-APSK

FIG. 140

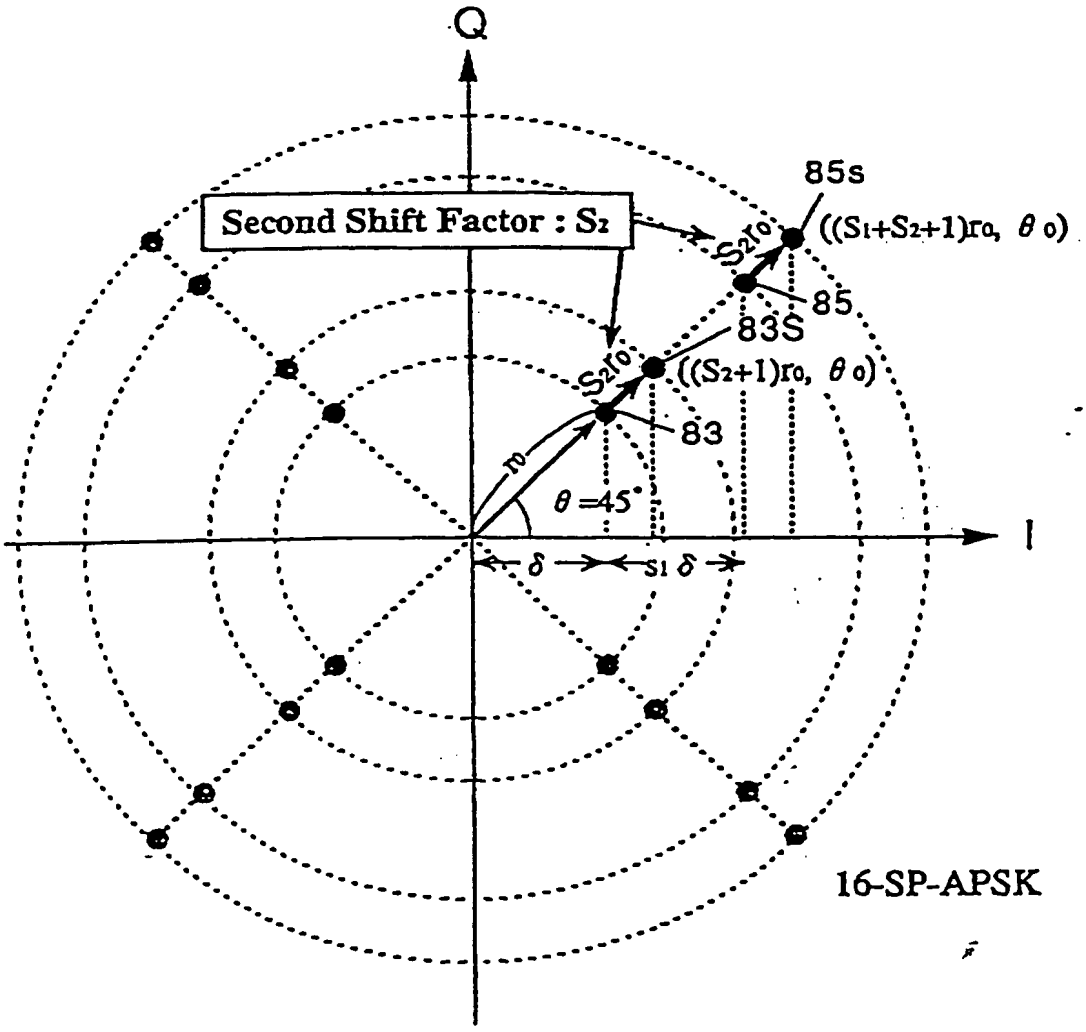

Q
I
Second Shift Factor : S2
85s
((S1+S2+1)r0, θ0)
85
83S
((S2+1)r0, θ0)
83
S2r0
r0
θ=45°
δ
S1 δ
16-SP-APSK

FIG. 141

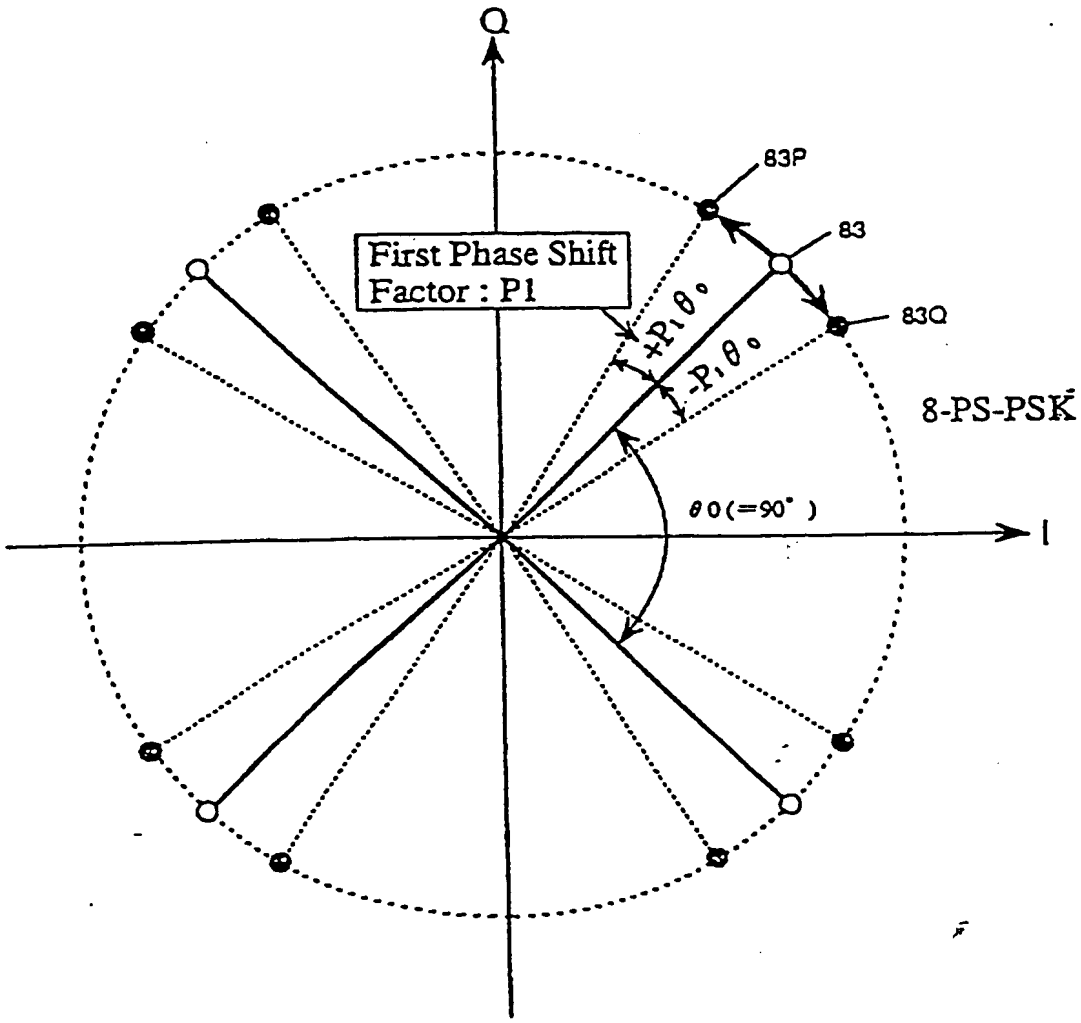


FIG. 142

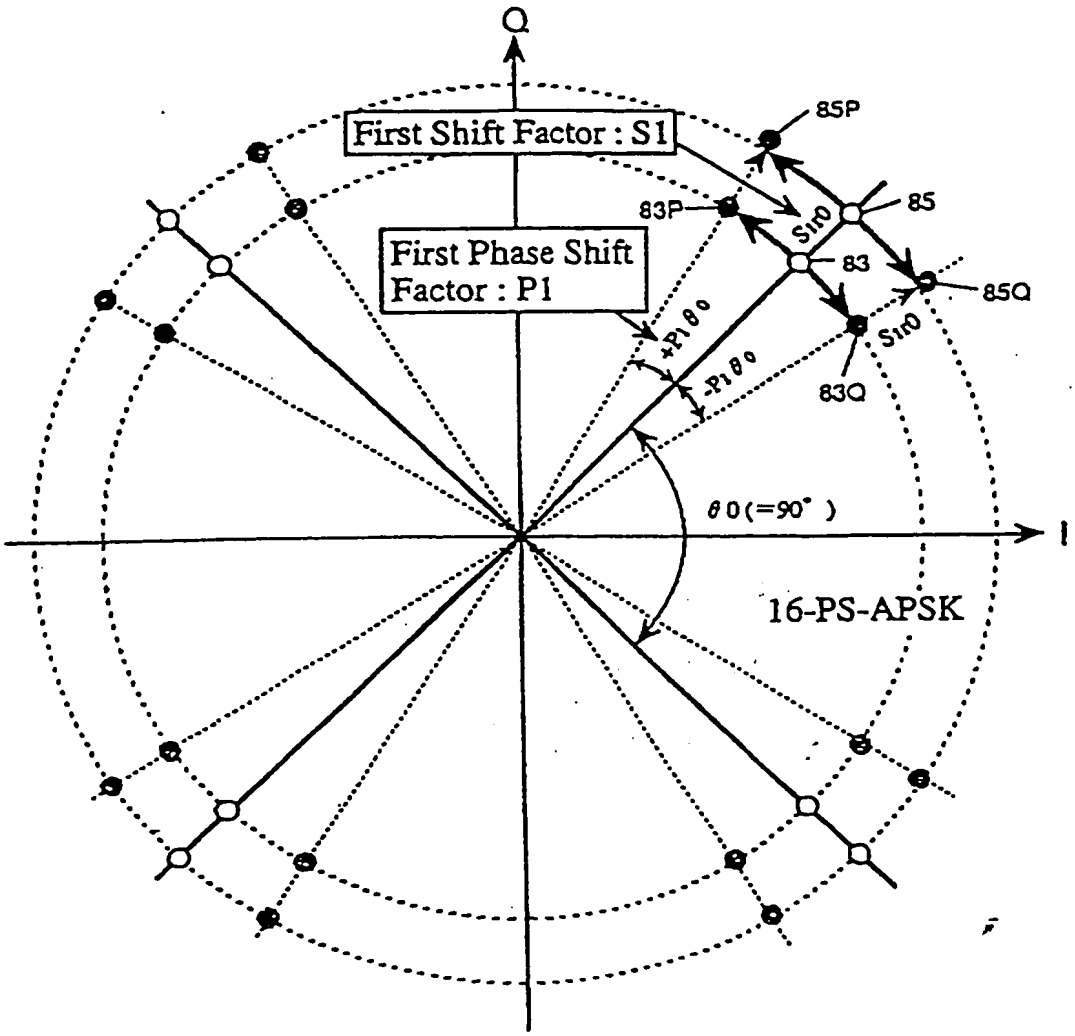

Q
First Shift Factor : S1
First Phase Shift Factor : P1
85P
85
83P
83
85Q
83Q
S1r0
+P1θ0
-P1θ0
θ0(=90°)
I
16-PS-APSK

FIG. 143

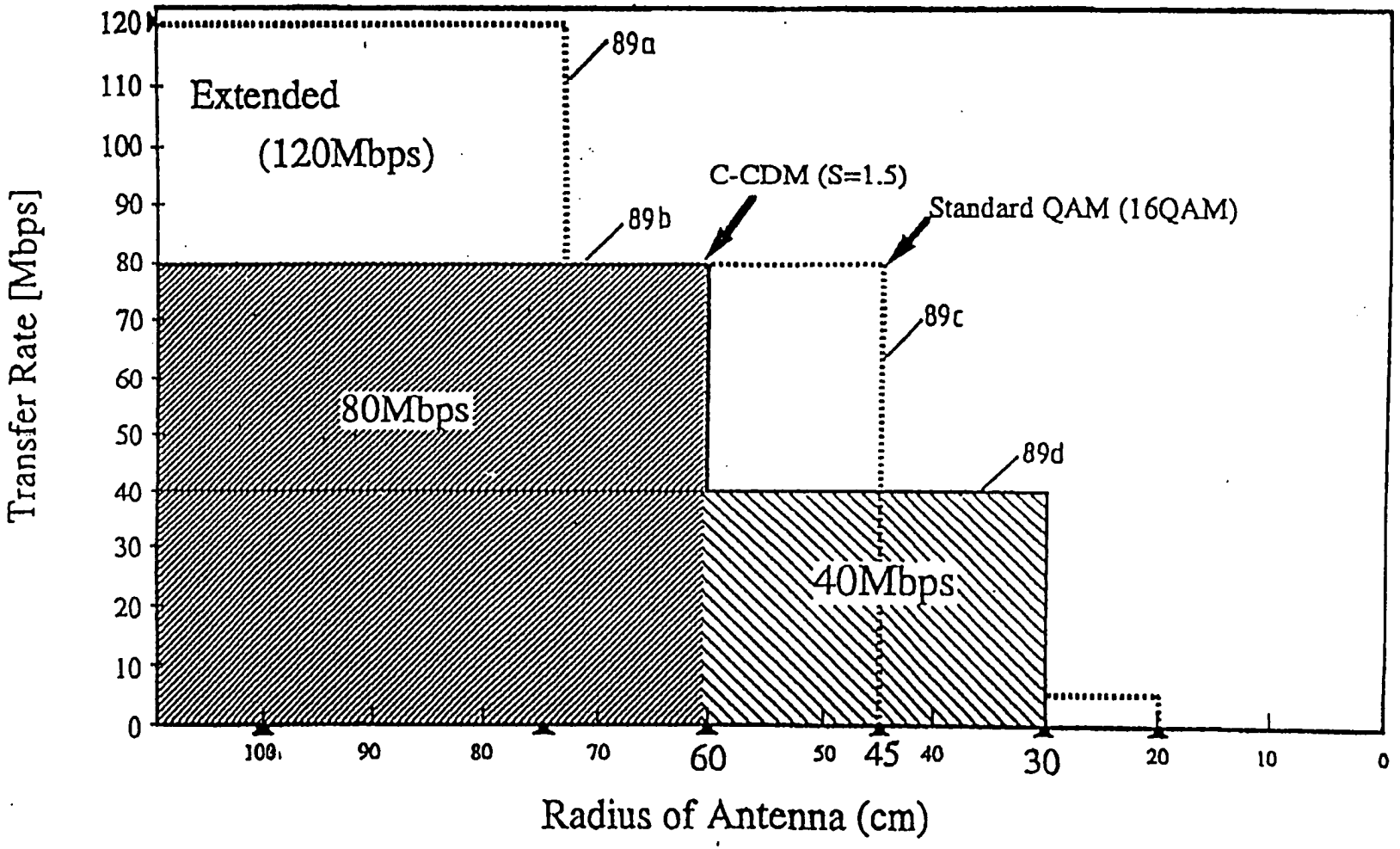

Transfer Rate [Mbps]
120
110
100
90
80
70
60
50
40
30
20
10
0
Extended
(120Mbps)
89a
89b
C-CDM (S=1.5)
Standard QAM (16QAM)
89c
89d
80Mbps
40Mbps
100
90
80
70
60
50
45
40
30
20
10
0
Radius of Antenna (cm)

FIG. 144

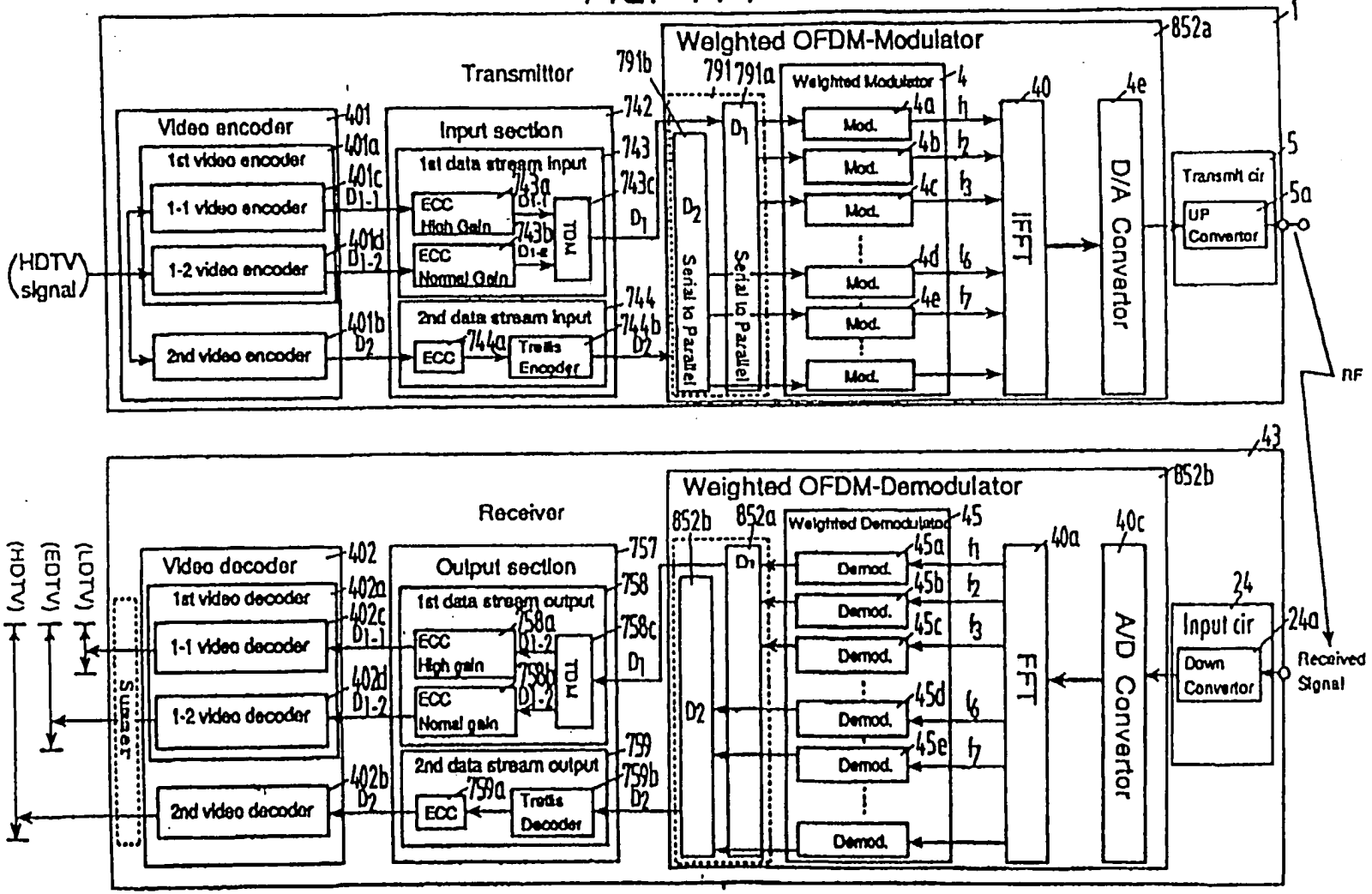

Transmitter
Weighted OFDM-Modulator
Video encoder
1st video encoder
1-1 video encoder
1-2 video encoder
2nd video encoder
Input section
1st data stream input
2nd data stream input
ECC
High Gain
Normal Gain
TDM
Trellis Encoder
Weighted Modulator
Mod.
IFFT
D/A Convertor
Transmit cir
UP Convertor
Serial to Parallel
(HDTV) signal
RF
Receiver
Weighted OFDM-Demodulator
Video decoder
1st video decoder
1-1 video decoder
1-2 video decoder
2nd video decoder
Output section
1st data stream output
2nd data stream output
Trellis Decoder
Weighted Demodulator
Demod.
FFT
A/D Convertor
Input cir
Down Convertor
Received Signal
Sumer
(HDTV)
(EDTV)
(LDTV)

FIG. 145(a)

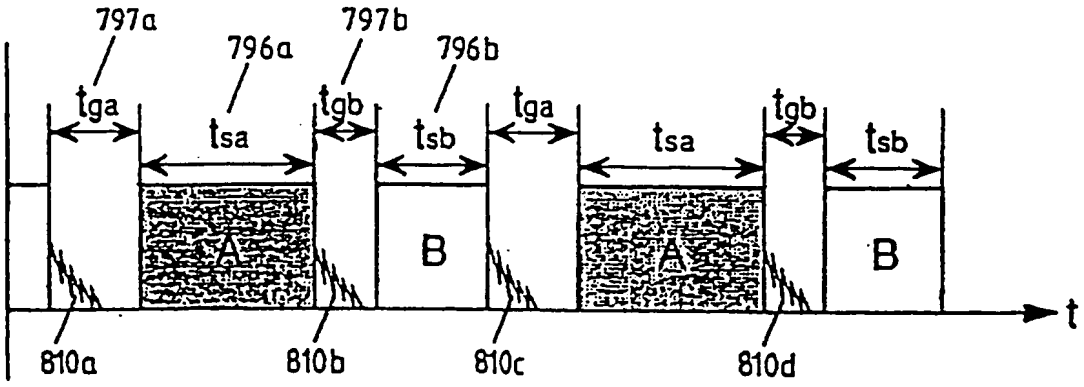


FIG. 145(b)

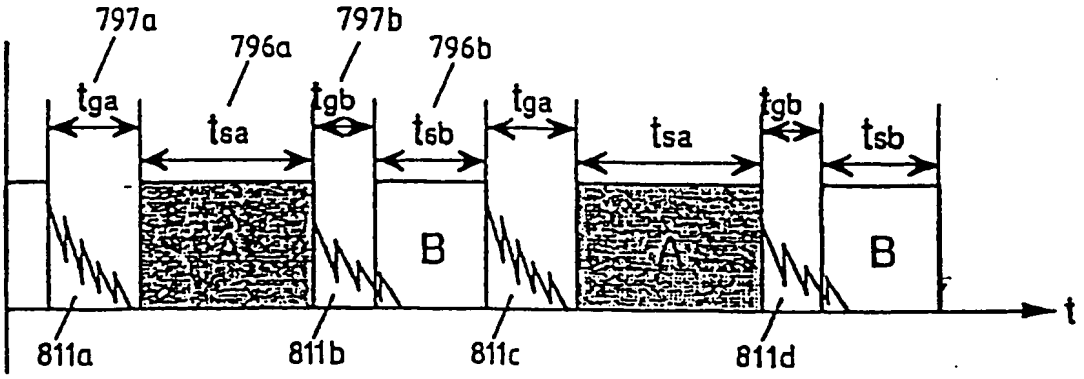
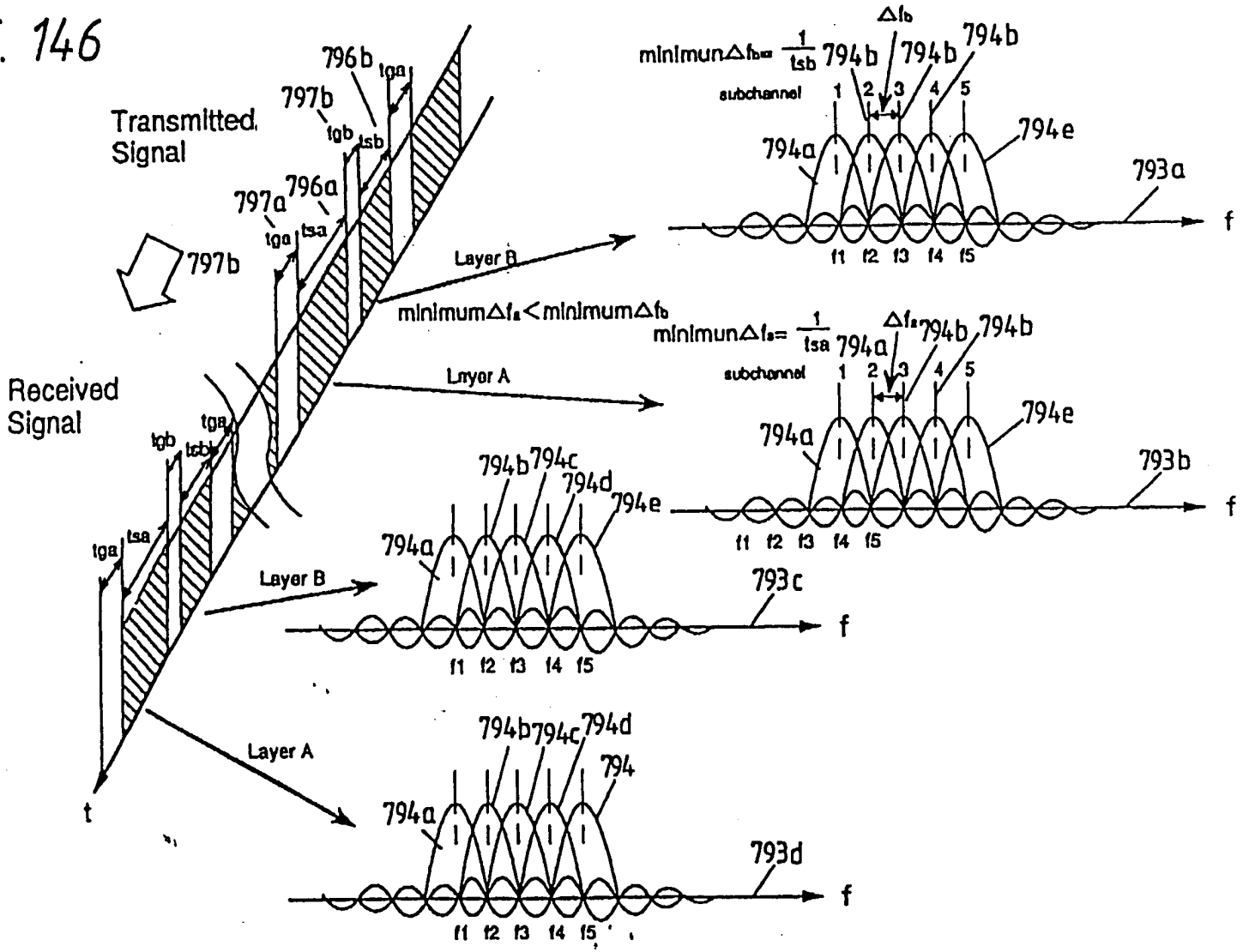


FIG. 146


Transmitted Signal
Received Signal
797b
797a
796b
796a
tga
tgb
tsb
tsa
Layer B
Layer A
minimumΔf_b = $\frac{1}{t_{sb}}$
minimumΔf_a = $\frac{1}{t_{sa}}$
minimumΔf_a < minimumΔf_b
Δf_b
Δf_a
subchannel
1 2 3 4 5
794a
794b
794c
794d
794e
794
793a
793b
793c
793d
f
t
f1 f2 f3 f4 f5

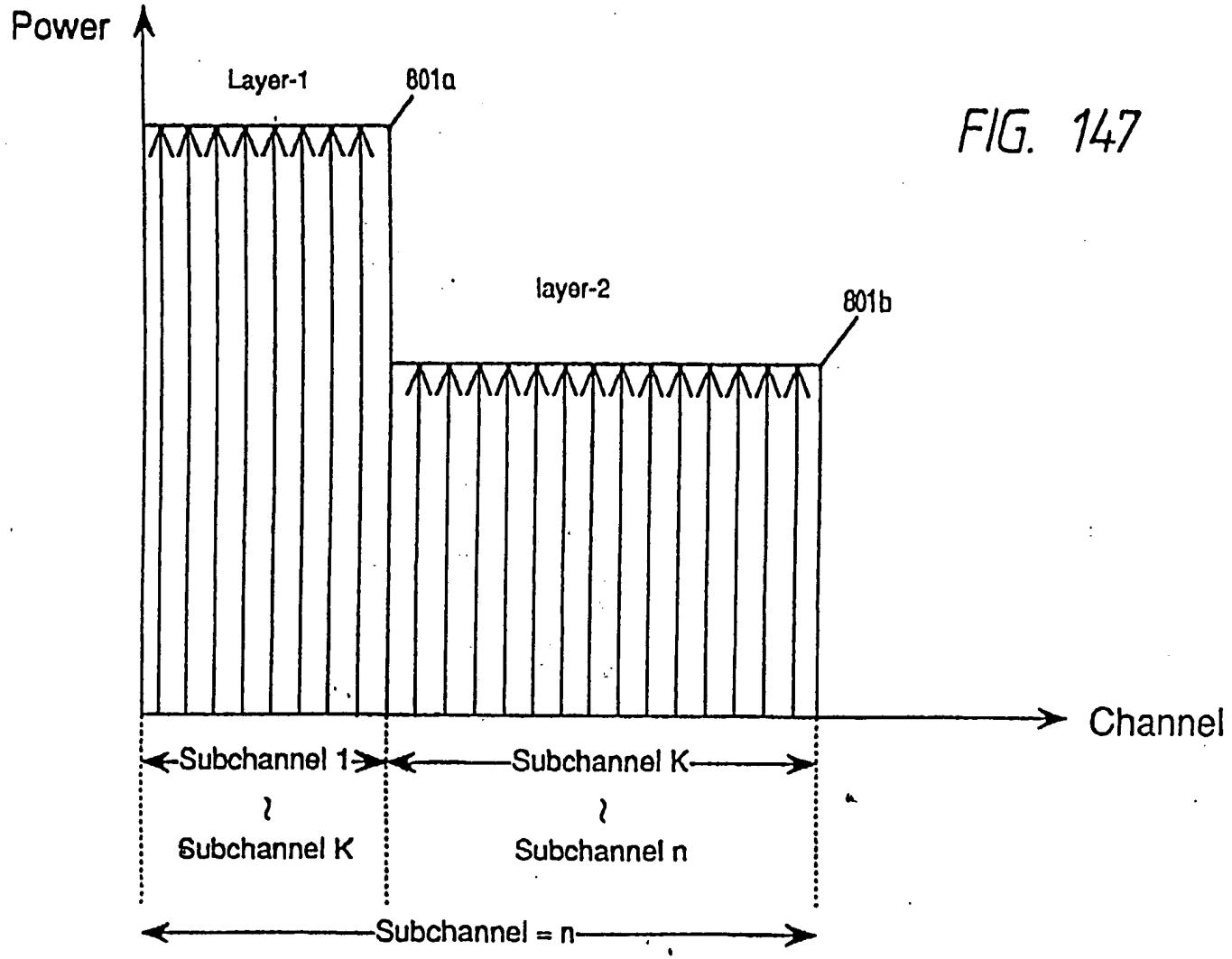

Power
Layer-1
801a
layer-2
801b
Channel
Subchannel 1
Subchannel K
Subchannel K
Subchannel n
Subchannel = n

FIG. 147

FIG. 148

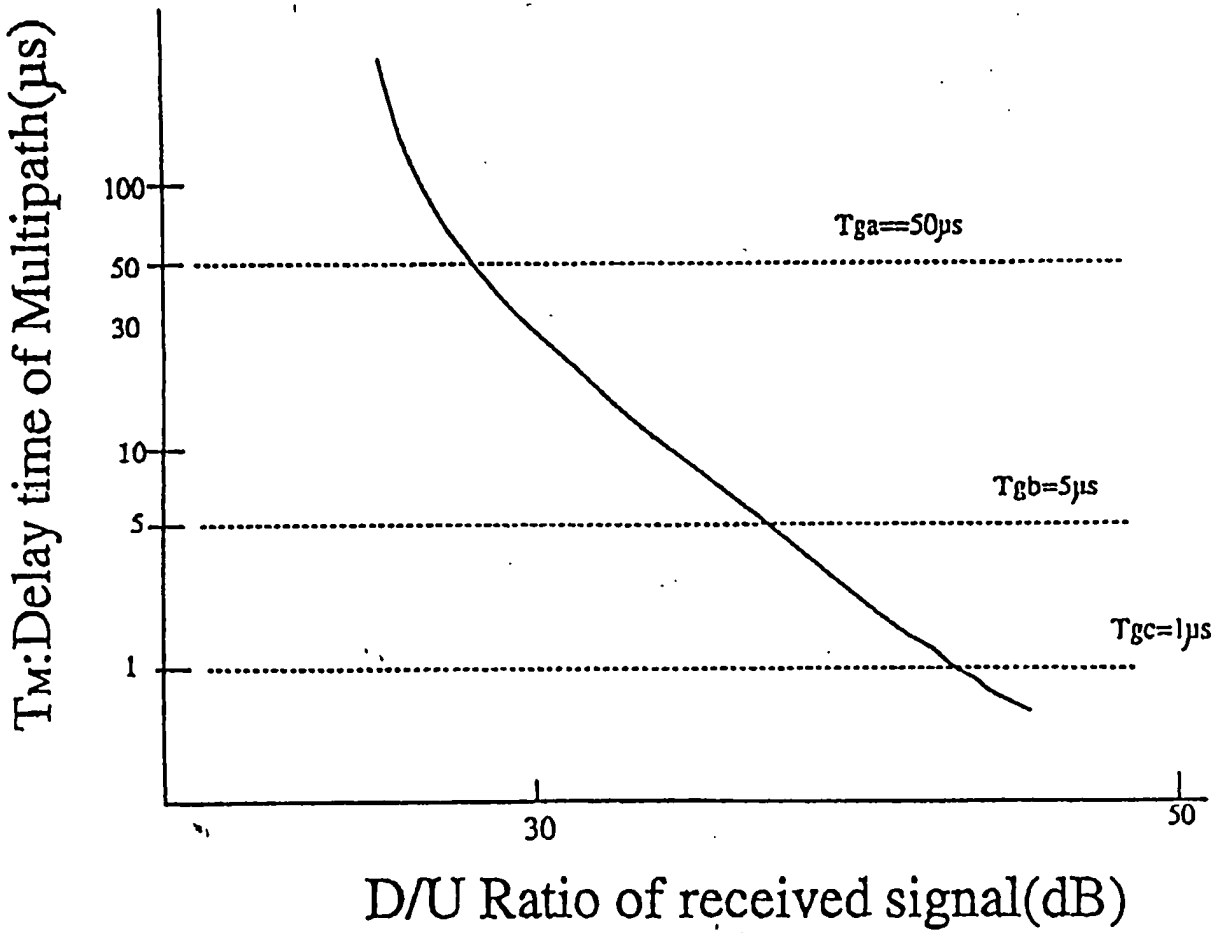

TM:Delay time of Multipath(μs)
100
50
30
10
5
1
Tga==50μs
Tgb=5μs
Tgc=1μs
30
50
D/U Ratio of received signal(dB)

FIG. 149(a)

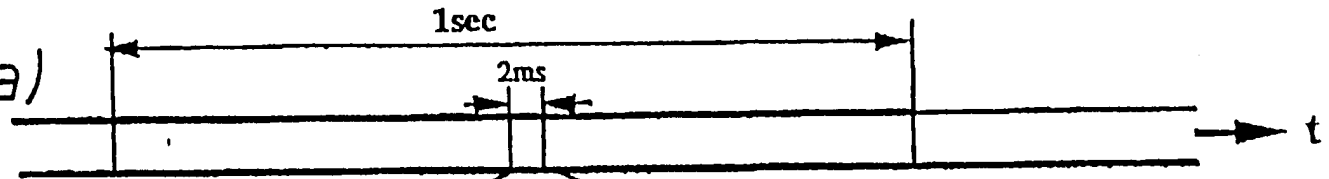


FIG. 149(b)

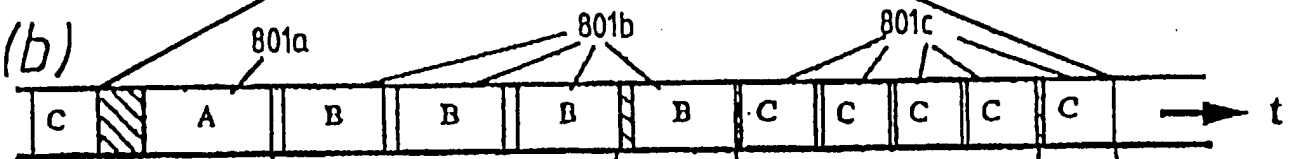


FIG. 149(c)

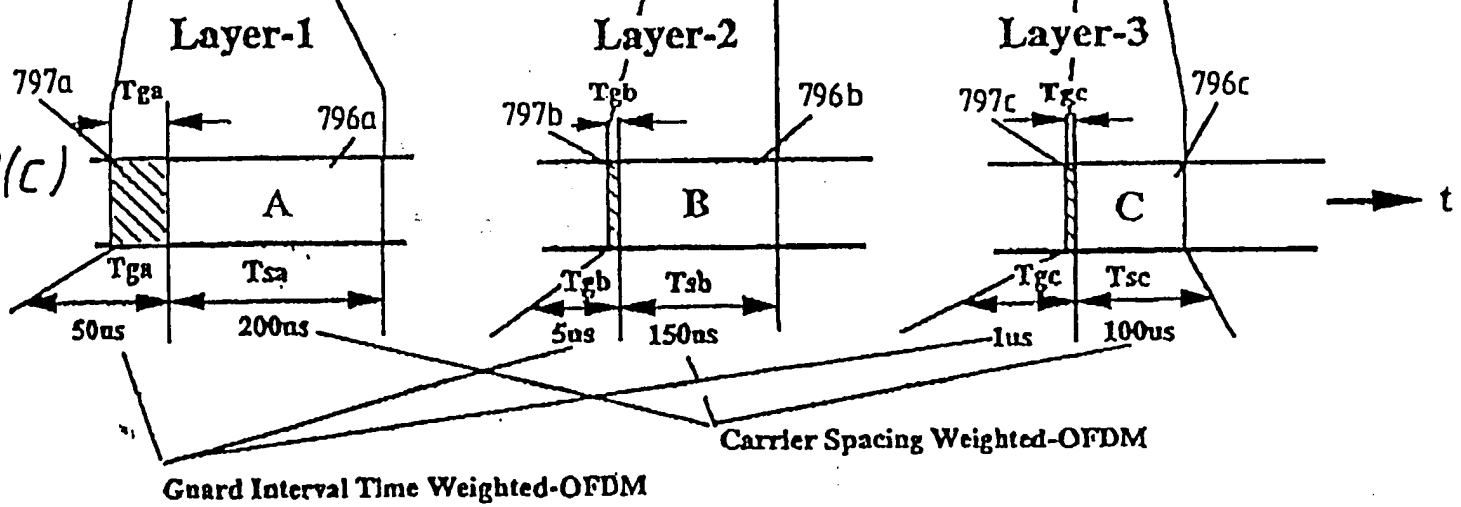


FIG. 150

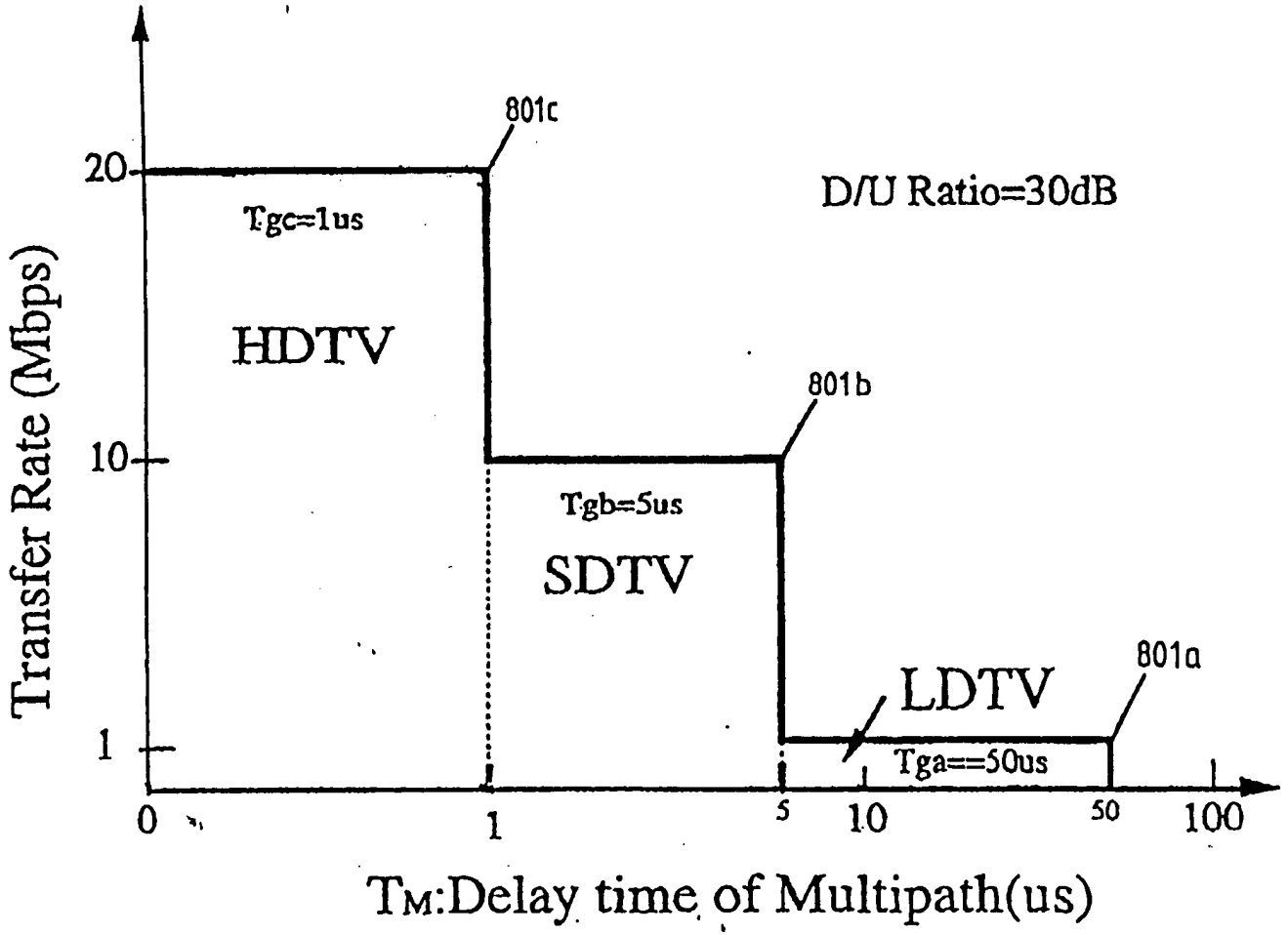

801c
20
Tgc=1us
D/U Ratio=30dB
HDTV
801b
10
Tgb=5us
SDTV
801a
LDTV
1
Tga==50us
Transfer Rate (Mbps)
0
1
5
10
50
100
TM:Delay time of Multipath(us)

FIG. 151

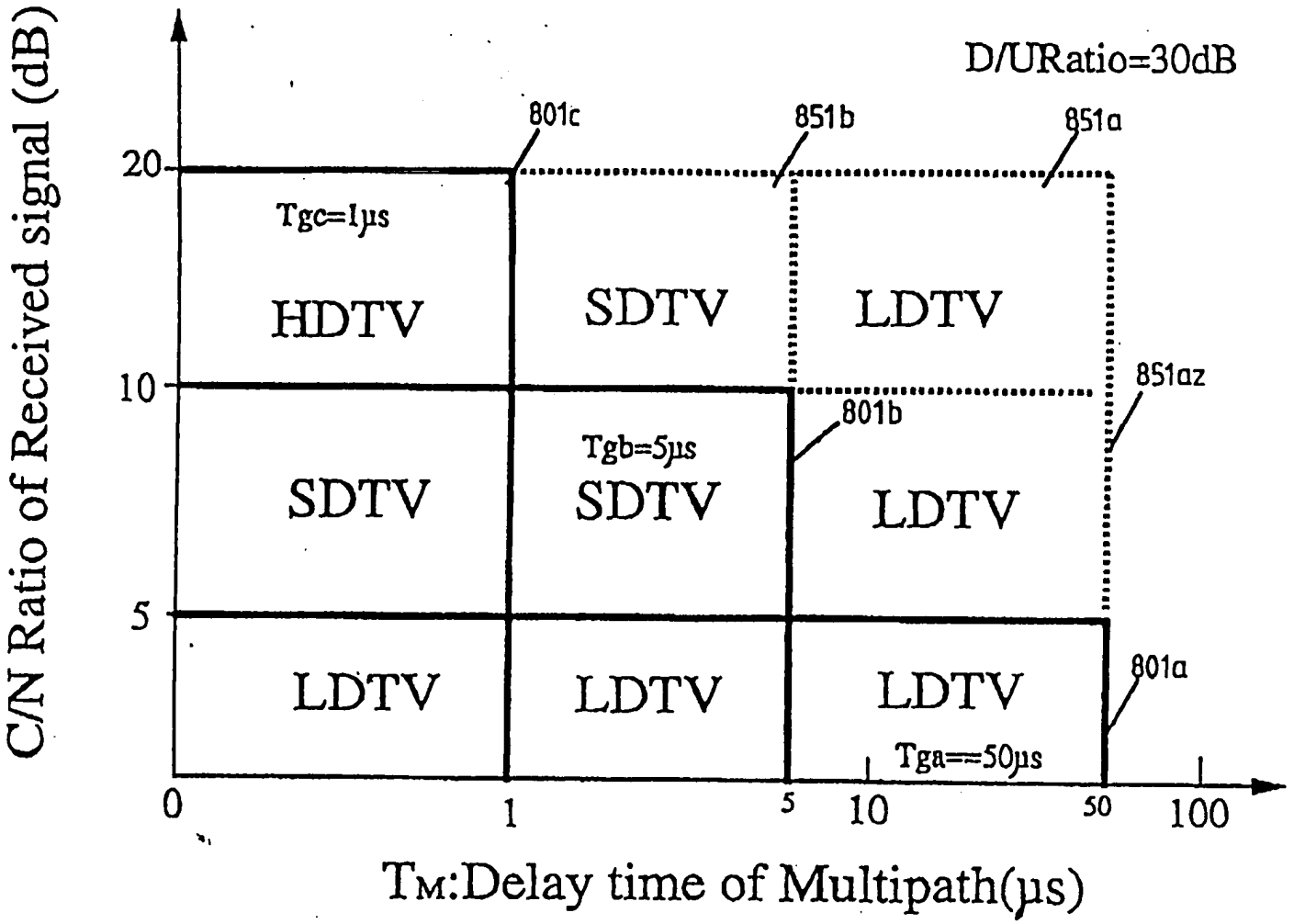

D/URatio=30dB
801c
851b
851a
851az
801b
801a
20
10
5
0
1
5
10
50
100
Tgc=1μs
Tgb=5μs
Tga=50μs
HDTV
SDTV
LDTV
SDTV
SDTV
LDTV
LDTV
LDTV
LDTV
C/N Ratio of Received signal (dB)
TM:Delay time of Multipath(μs)

FIG. 152

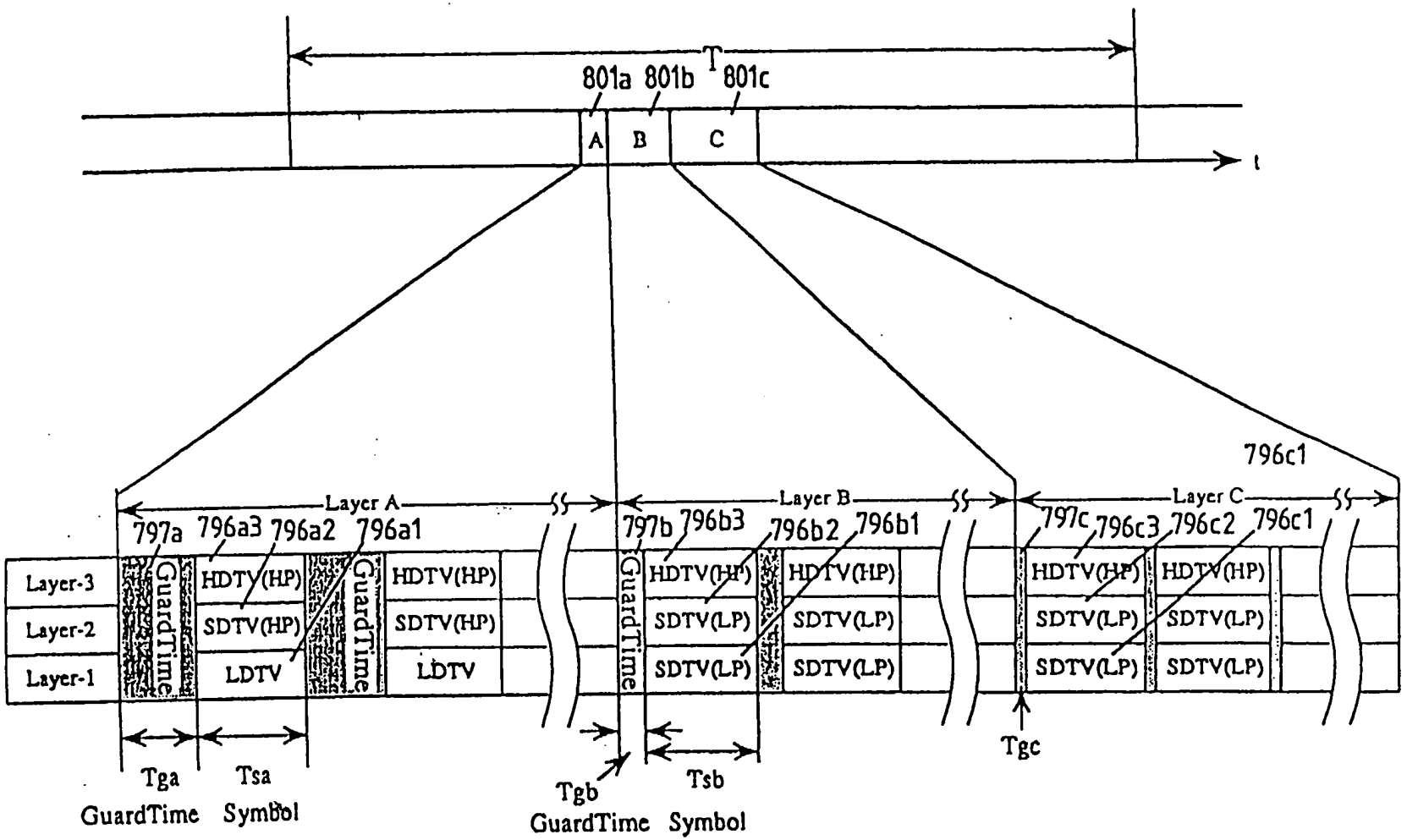

T
801a
801b
801c
A
B
C
t
796c1
Layer A
Layer B
Layer C
797a
796a3
796a2
796a1
797b
796b3
796b2
796b1
797c
796c3
796c2
796c1
Layer-3
Layer-2
Layer-1
GuardTime
HDTV(HP)
SDTV(HP)
LDTV
SDTV(LP)
Tga
Tsa
Tgb
Tsb
Tgc
GuardTime
Symbol

FIG. 153

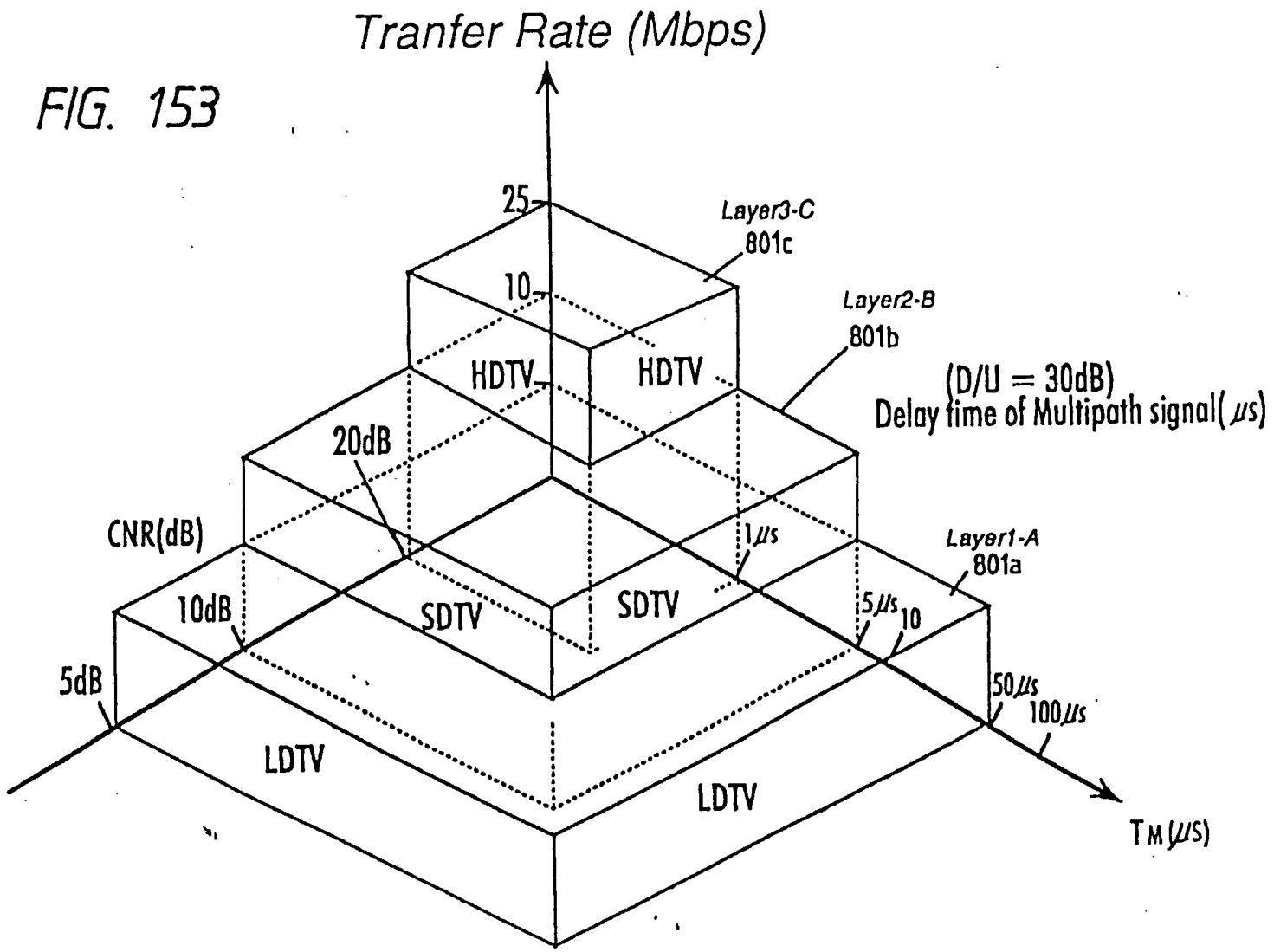

Tranfer Rate (Mbps)
25
10
Layer3-C
801c
Layer2-B
801b
HDTV
HDTV
(D/U = 30dB)
Delay time of Multipath signal(μs)
20dB
CNR(dB)
1μs
Layer1-A
801a
10dB
SDTV
SDTV
5μs
10
5dB
50μs
100μs
LDTV
LDTV
TM(μs)

FIG. 154

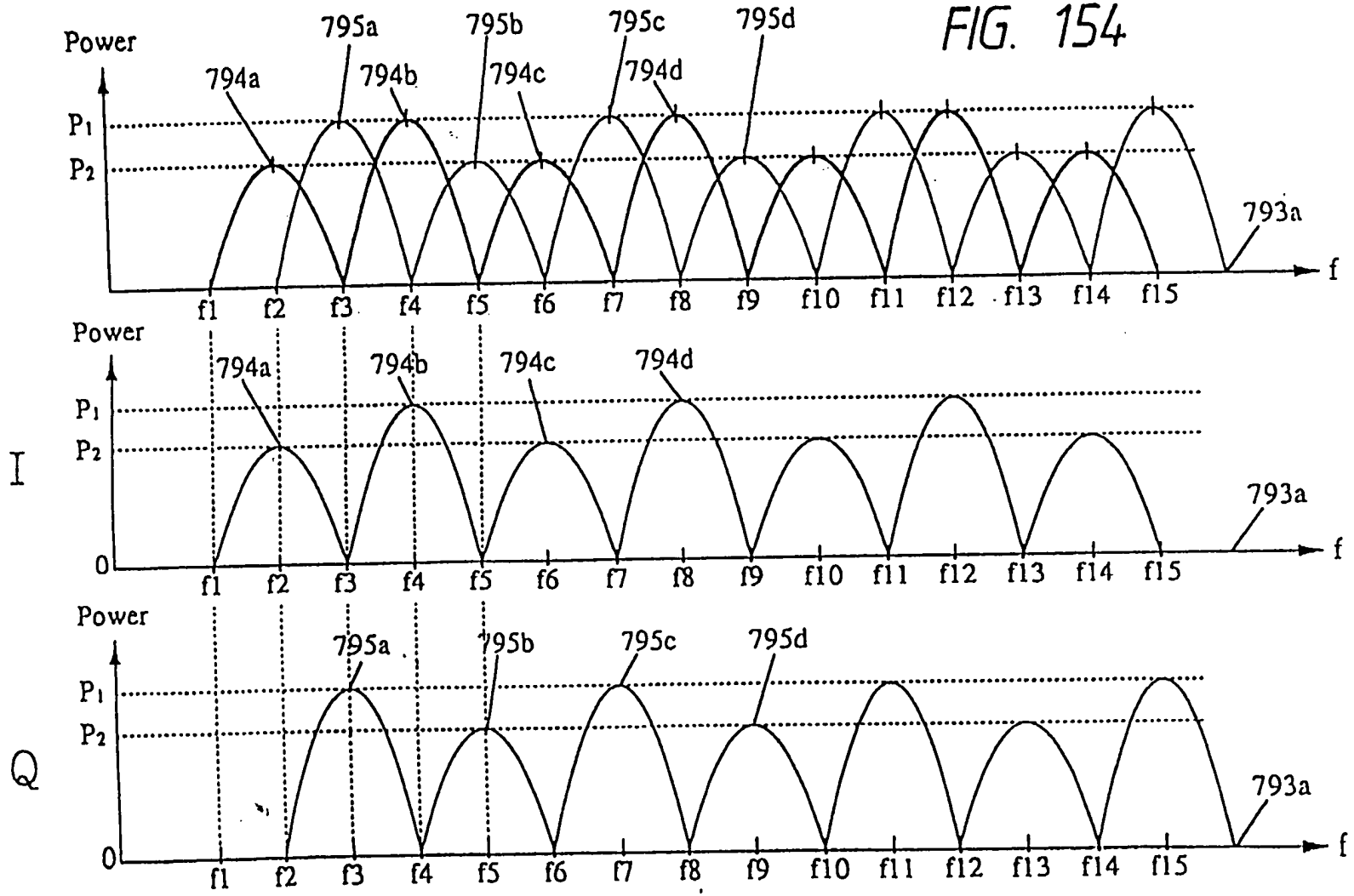

Power
795a
795b
795c
795d
794a
794b
794c
794d
P1
P2
793a
f
f1
f2
f3
f4
f5
f6
f7
f8
f9
f10
f11
f12
f13
f14
f15
I
Power
794a
794b
794c
794d
P1
P2
0
793a
f
f1
f2
f3
f4
f5
f6
f7
f8
f9
f10
f11
f12
f13
f14
f15
Power
795a
795b
795c
795d
P1
P2
Q
0
793a
f
f1
f2
f3
f4
f5
f6
f7
f8
f9
f10
f11
f12
f13
f14
f15

FIG. 155

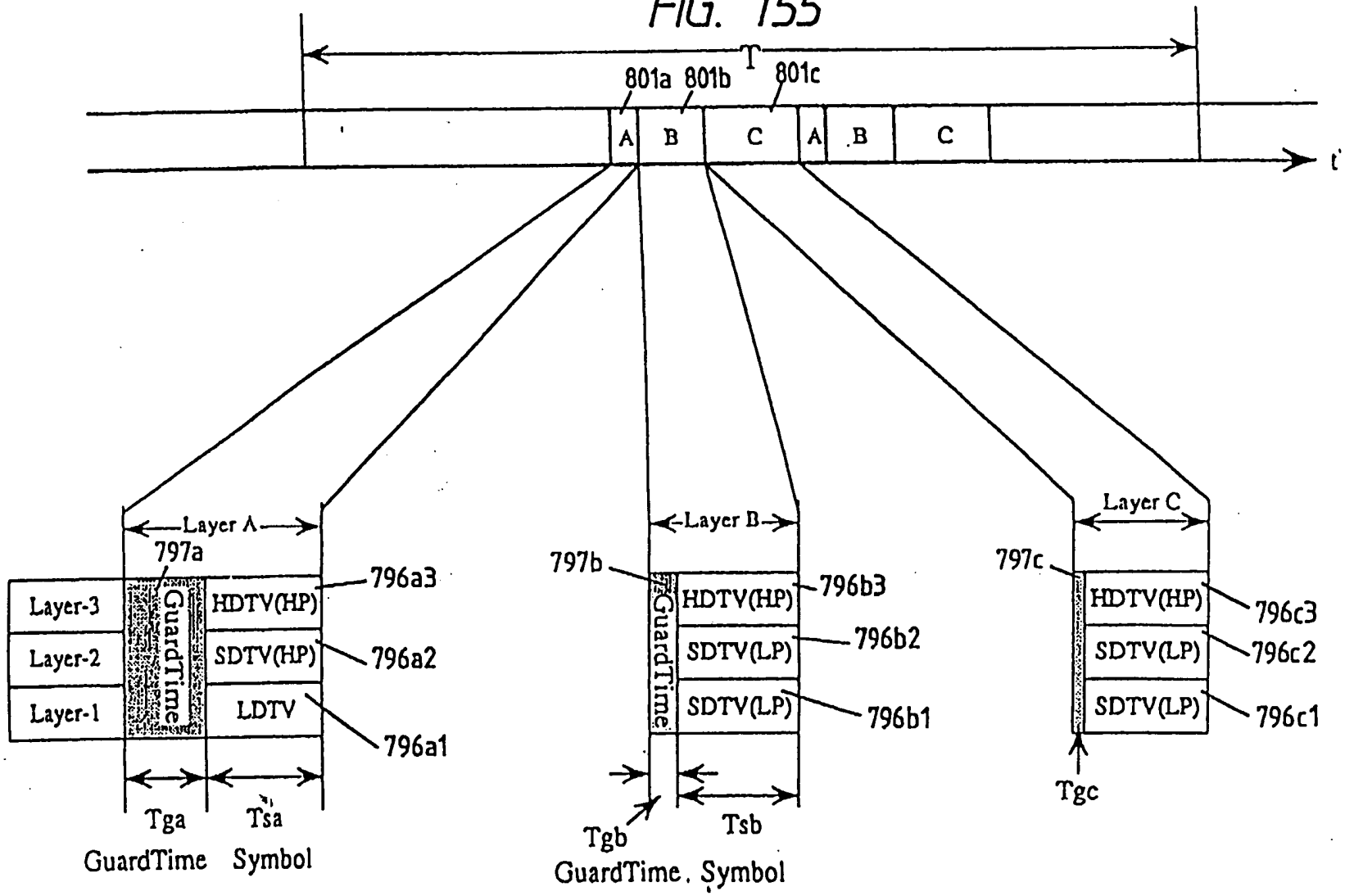

T
801a
801b
801c
A
B
C
A
B
C
t
Layer A
797a
Layer-3
Layer-2
Layer-1
GuardTime
HDTV(HP)
SDTV(HP)
LDTV
796a3
796a2
796a1
Tga
Tsa
GuardTime
Symbol
Layer B
797b
GuardTime
HDTV(HP)
SDTV(LP)
SDTV(LP)
796b3
796b2
796b1
Tgb
Tsb
GuardTime
Symbol
Layer C
797c
HDTV(HP)
SDTV(LP)
SDTV(LP)
796c3
796c2
796c1
Tgc

FIG. 156

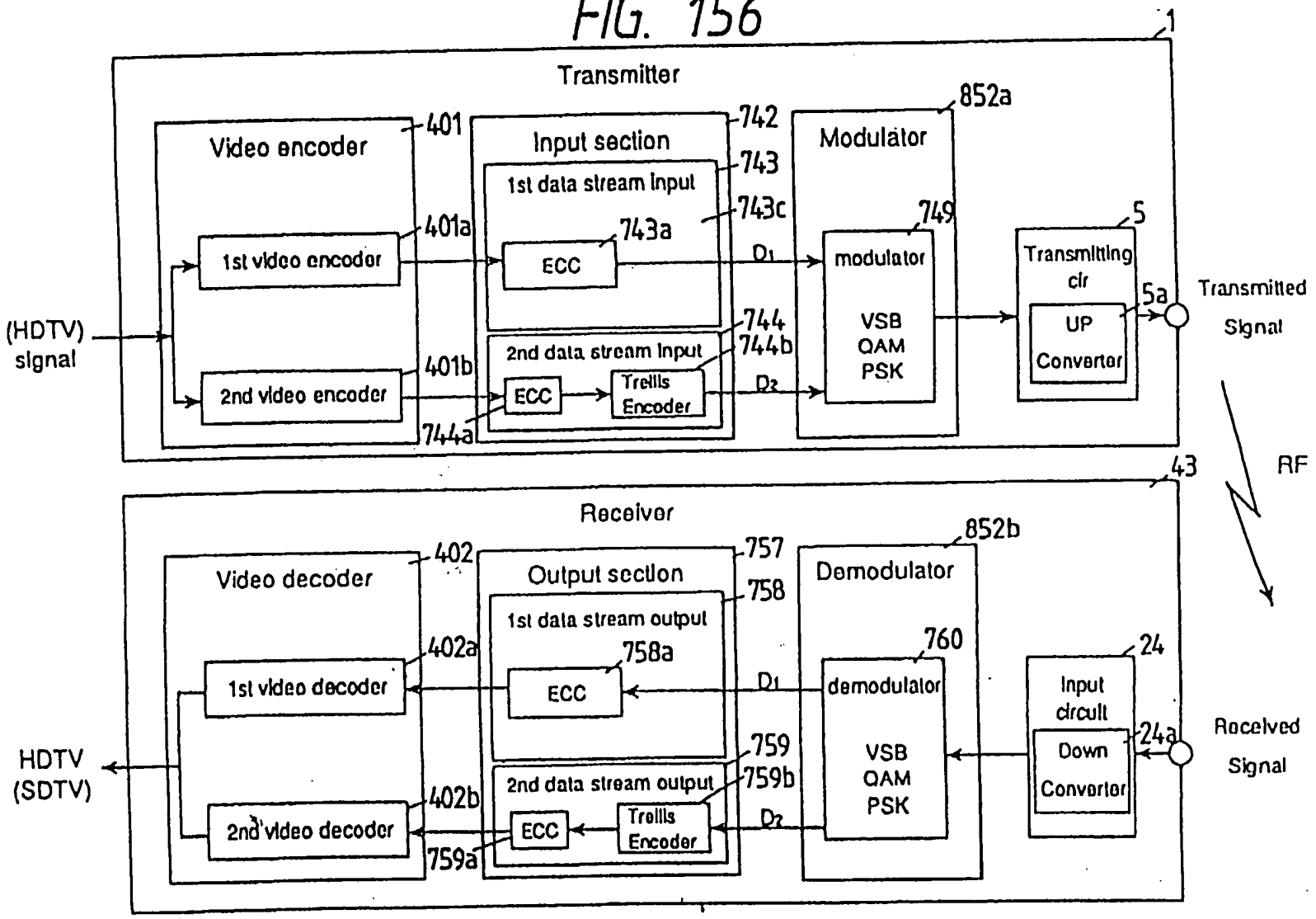

1
Transmitter
Video encoder
401
1st video encoder
401a
2nd video encoder
401b
(HDTV) signal
Input section
742
1st data stream input
743
743a
ECC
743c
2nd data stream input
744
744b
ECC
Trellis Encoder
744a
D1
D2
Modulator
852a
749
modulator
VSB QAM PSK
Transmitting cir
5
UP Converter
5a
Transmitted Signal
RF
43
Receiver
Video decoder
402
1st video decoder
402a
2nd video decoder
402b
HDTV (SDTV)
Output section
757
1st data stream output
758
758a
ECC
2nd data stream output
759
759b
ECC
Trellis Encoder
759a
Demodulator
852b
760
demodulator
VSB QAM PSK
Input circuit
24
Down Converter
24a
Received Signal

FIG. 157

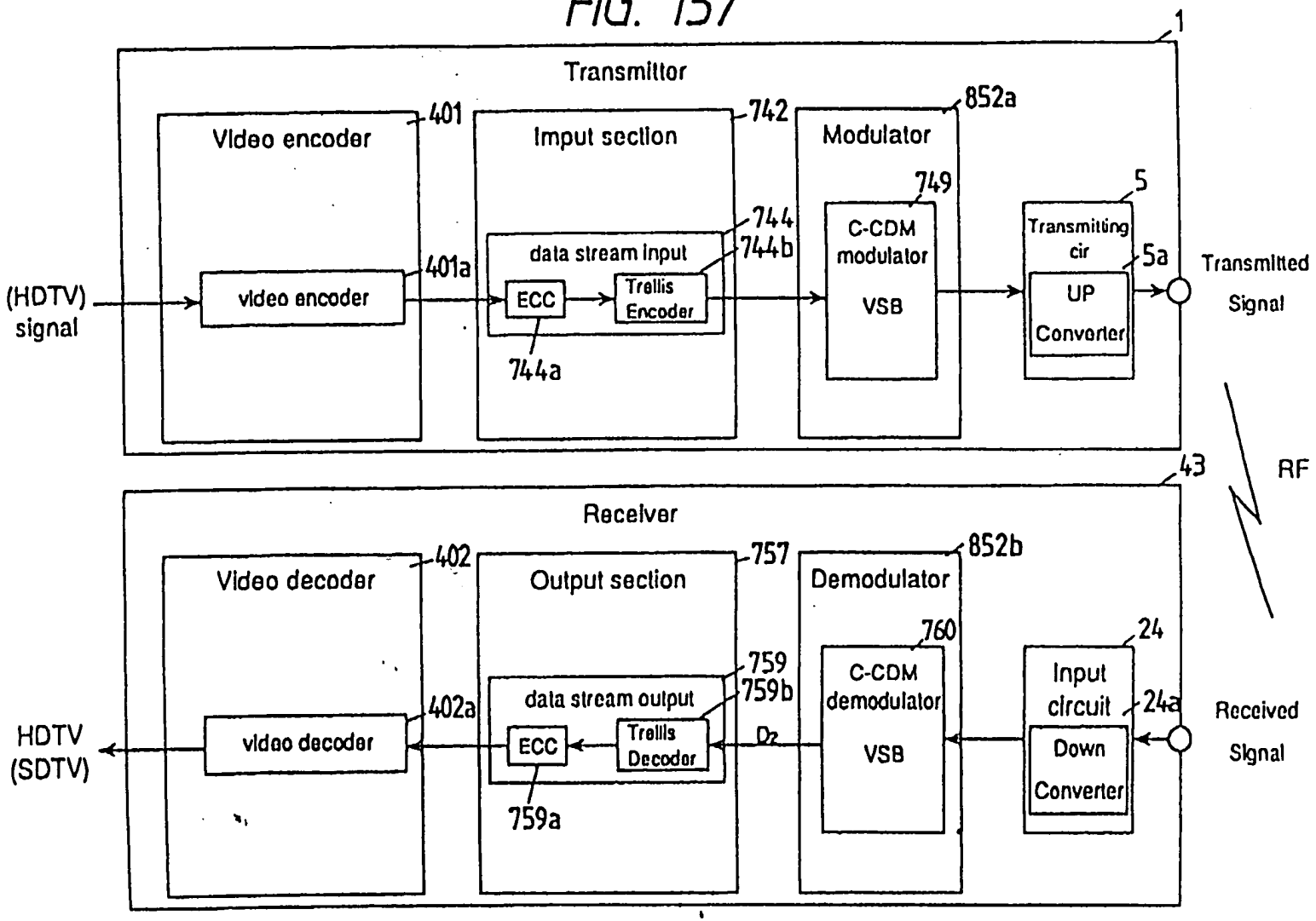

1
Transmittor
Video encoder
401
Input section
742
Modulator
852a
749
5
744
744b
data stream input
C-CDM modulator
VSB
Transmitting cir
5a
401a
(HDTV) signal
video encoder
ECC
Trellis Encoder
UP Converter
Transmitted Signal
744a
43
RF
Receiver
Video decoder
402
Output section
757
Demodulator
852b
760
24
759
759b
data stream output
C-CDM demodulator
Input circuit
402a
HDTV (SDTV)
video decoder
ECC
Trellis Decoder
VSB
Down Converter
24a
Received Signal
759a

FIG. 158

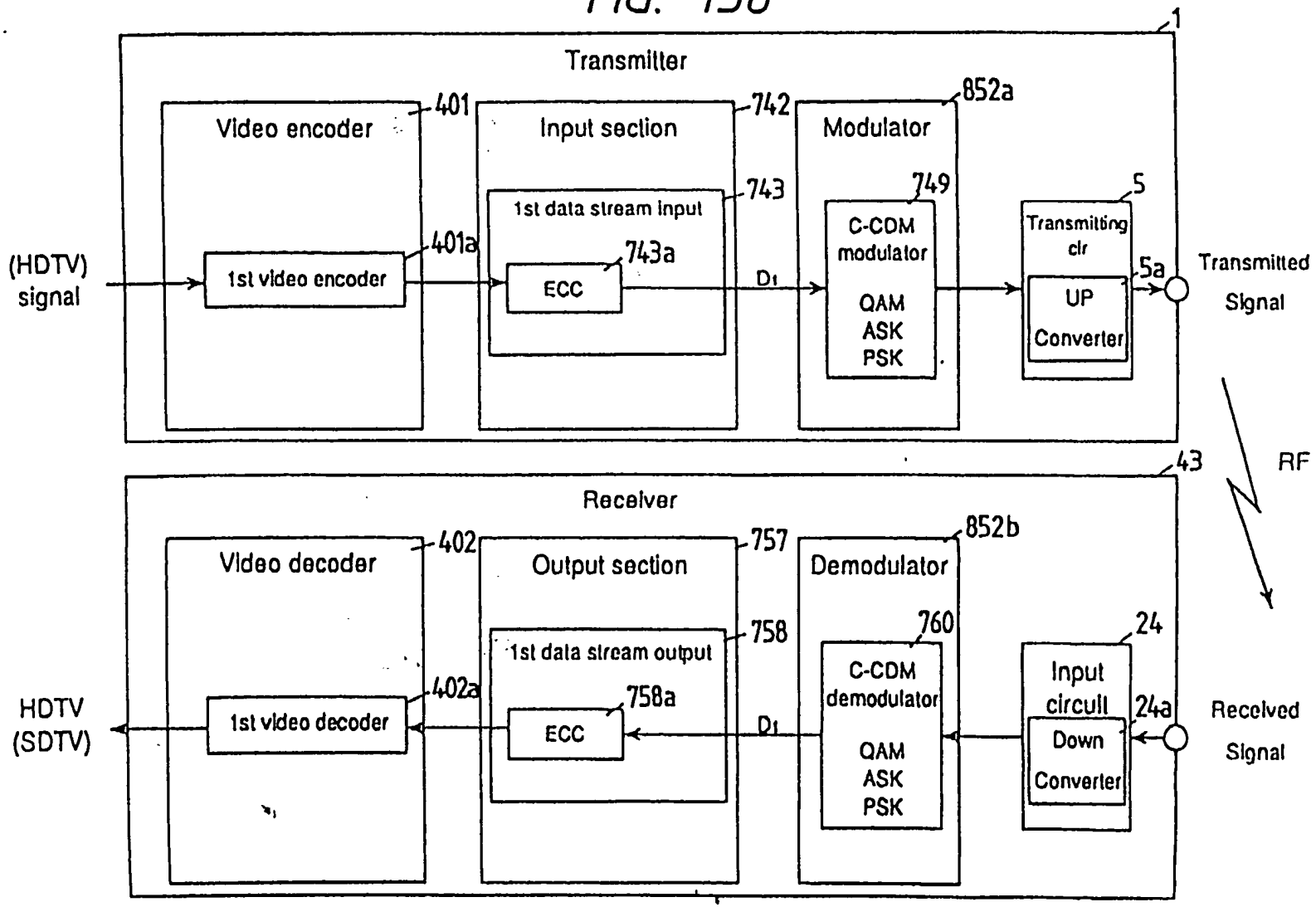

1
Transmitter
Video encoder
401
Input section
742
Modulator
852a
1st data stream input
743
749
5
C-CDM modulator
QAM
ASK
PSK
Transmitting clr
UP Converter
5a
(HDTV) signal
1st video encoder
401a
ECC
743a
D1
Transmitted Signal
RF
43
Receiver
Video decoder
402
Output section
757
Demodulator
852b
1st data stream output
758
760
24
C-CDM demodulator
QAM
ASK
PSK
Input circuit
Down Converter
24a
HDTV (SDTV)
1st video decoder
402a
ECC
758a
D1
Received Signal

FIG. 159(a)

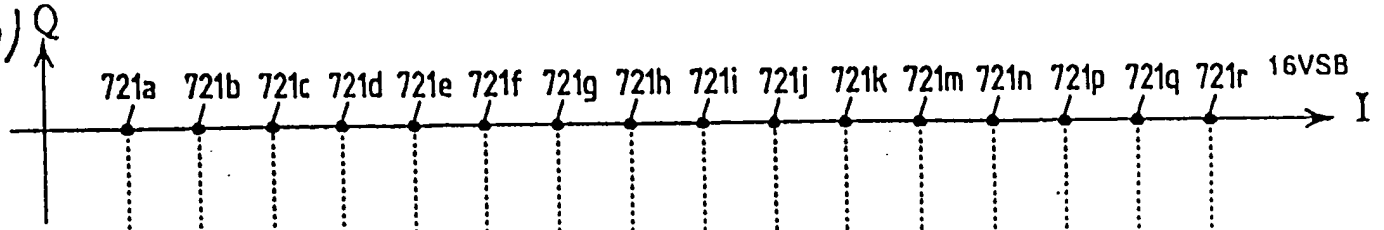


FIG. 159(b)

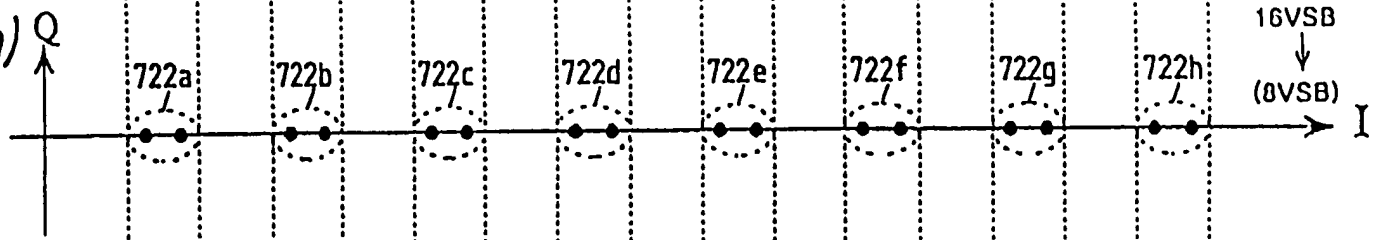


FIG. 159(c)

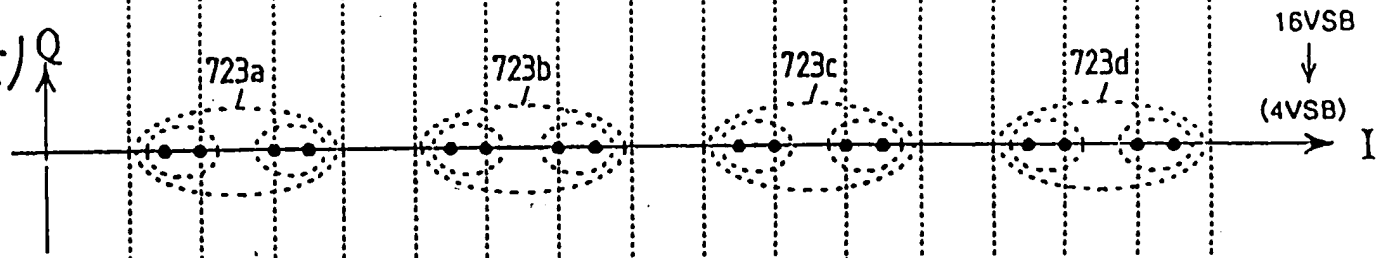


FIG. 159(d)

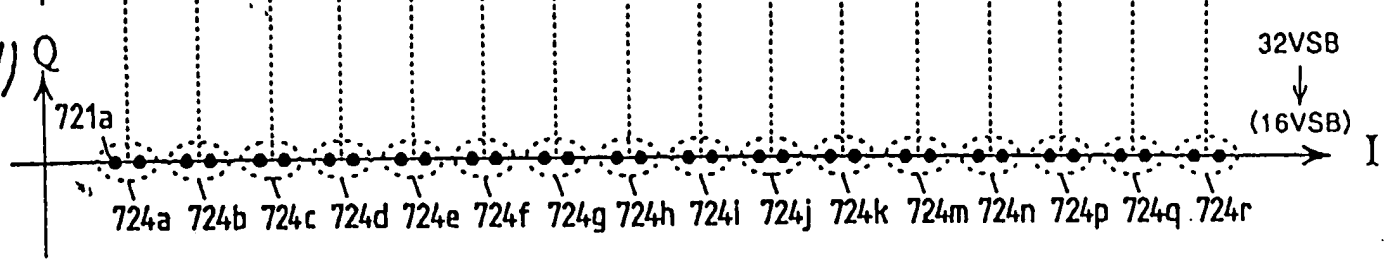


FIG. 160(a)

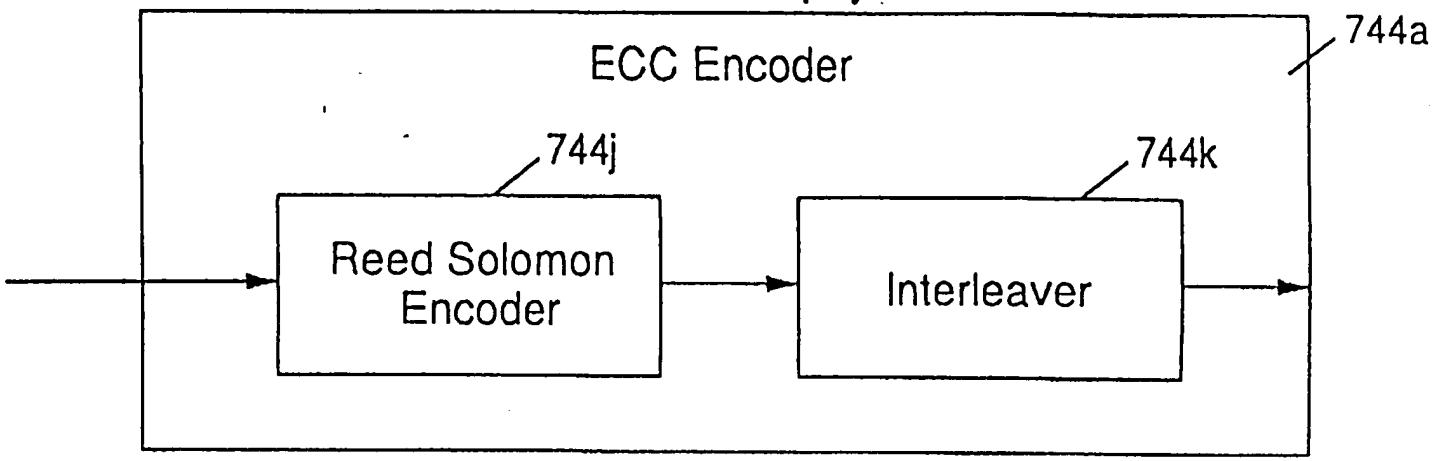


FIG. 160(b)

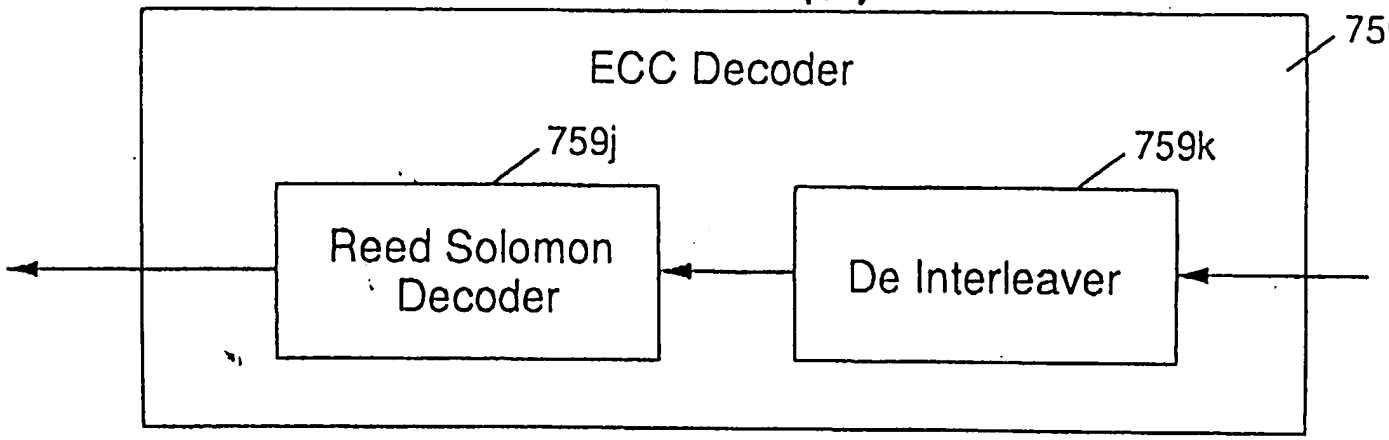


FIG. 161

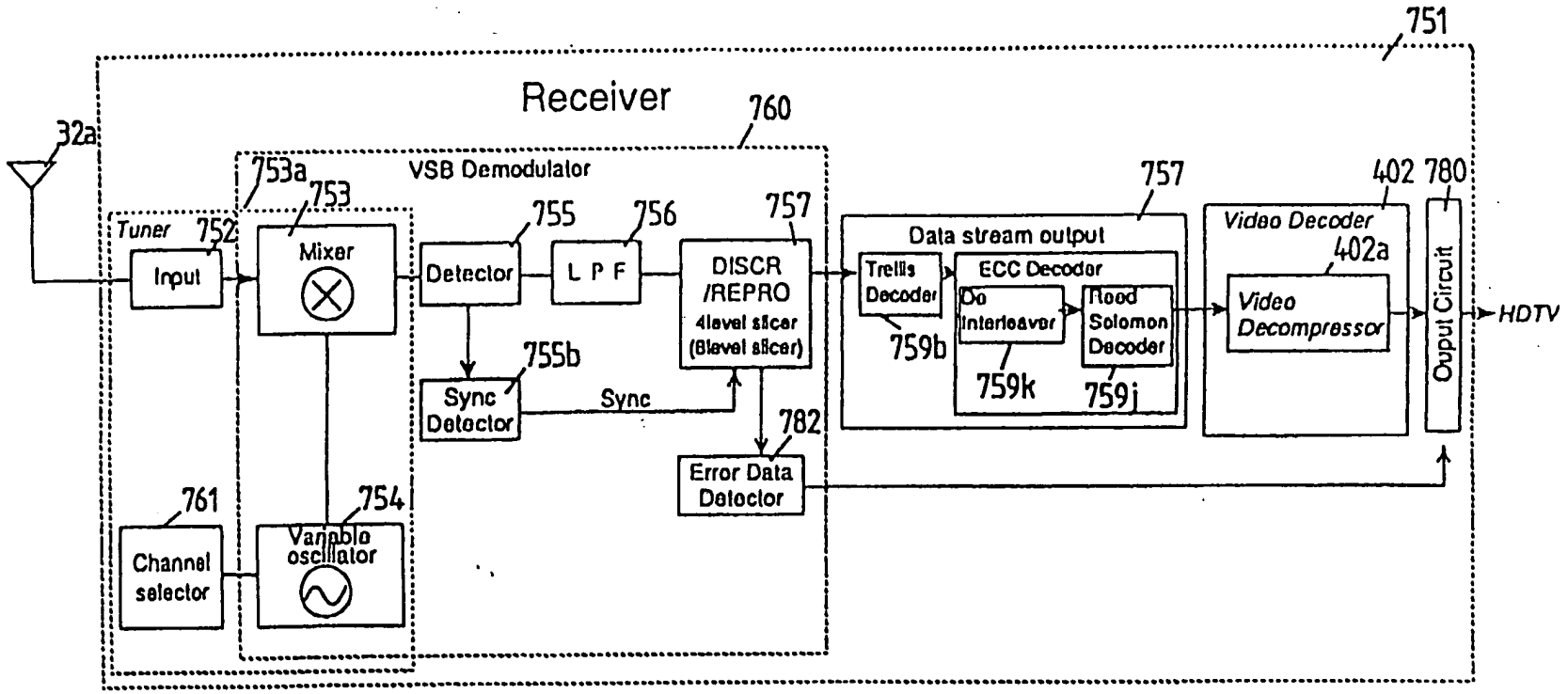

751
Receiver
760
32a
753a
VSB Demodulator
753
Tuner
752
Input
Mixer
Detector
755
L P F
756
DISCR
/REPRO
4level slicer
(8level slicer)
757
755b
Sync
Detector
Sync
782
Error Data
Detector
761
Channel
selector
754
Variable
oscillator
757
Data stream output
Trellis
Decoder
759b
ECC Decoder
De
Interleaver
759k
Read
Solomon
Decoder
759j
402
Video Decoder
402a
Video
Decompressor
780
Ouput Circuit
HDTV

FIG. 162

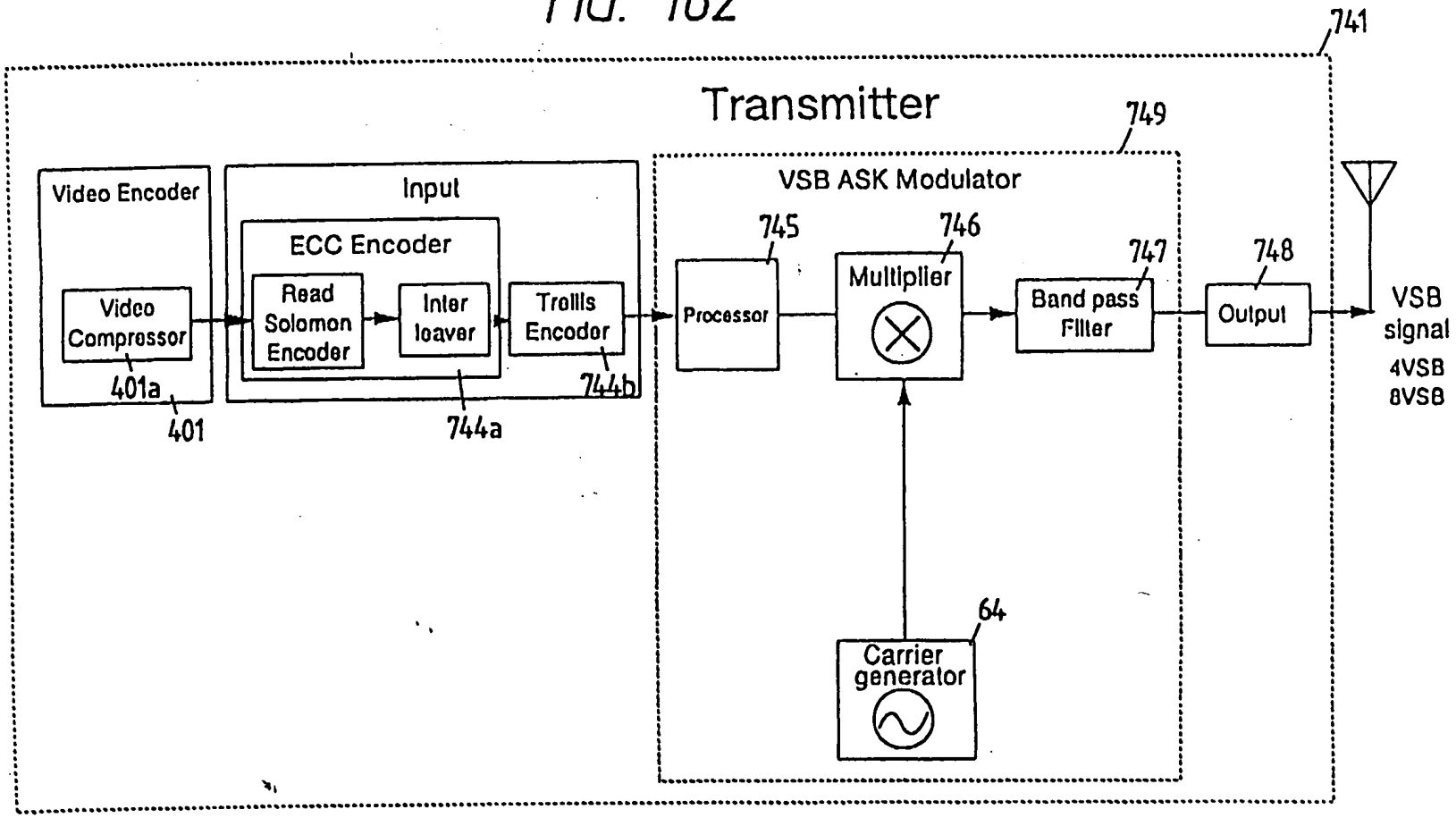

741
Transmitter
749
Video Encoder
Video Compressor
401a
401
Input
ECC Encoder
Read Solomon Encoder
Inter leaver
744a
Trellis Encoder
744b
VSB ASK Modulator
745
Processor
746
Multiplier
747
Band pass Filter
748
Output
VSB signal
4VSB
8VSB
64
Carrier generator

FIG. 163

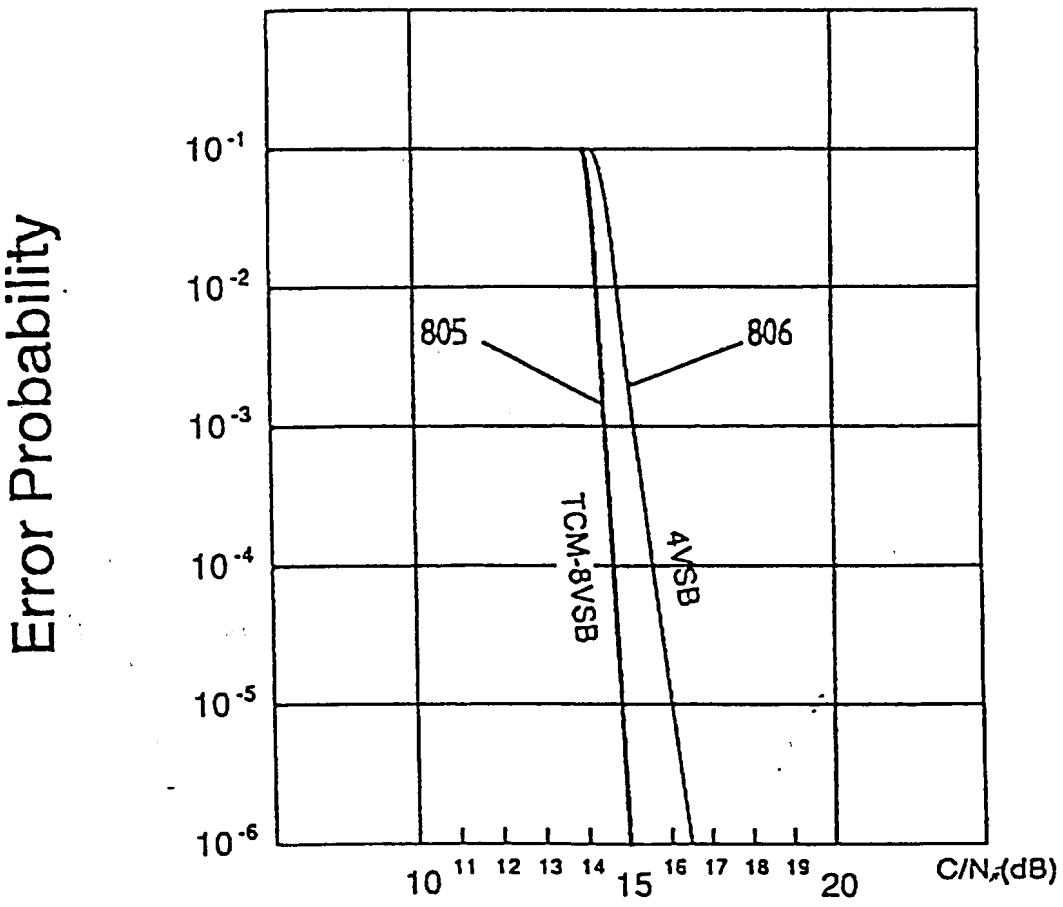

Error Probability
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
805
806
TCM-8VSB
4VSB
10 11 12 13 14 15 16 17 18 19 20
C/N (dB)

FIG. 164

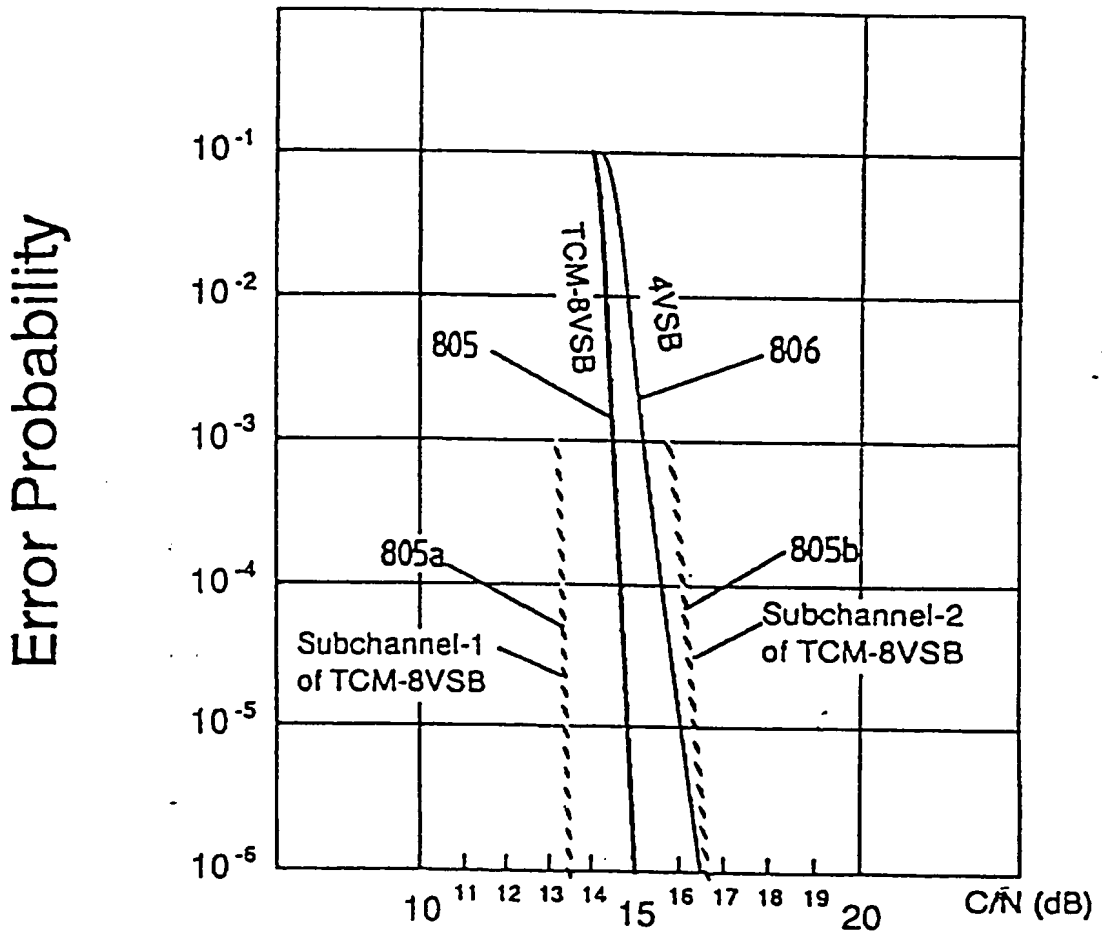

Error Probability
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
TCM-8VSB
4VSB
805
806
805a
805b
Subchannel-1
of TCM-8VSB
Subchannel-2
of TCM-8VSB
10 11 12 13 14 15 16 17 18 19 20
C/N (dB)

FIG. 165(a)

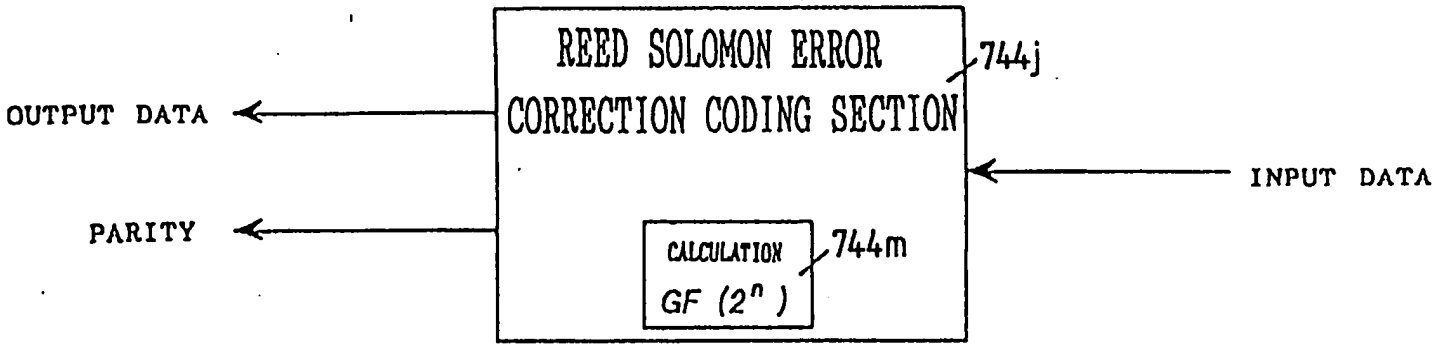


FIG. 165(b)

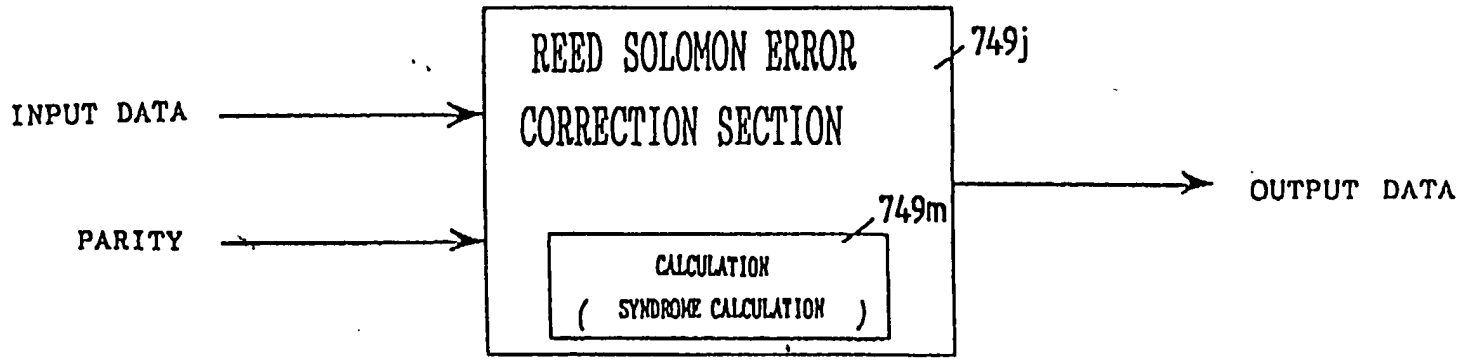


FIG. 166

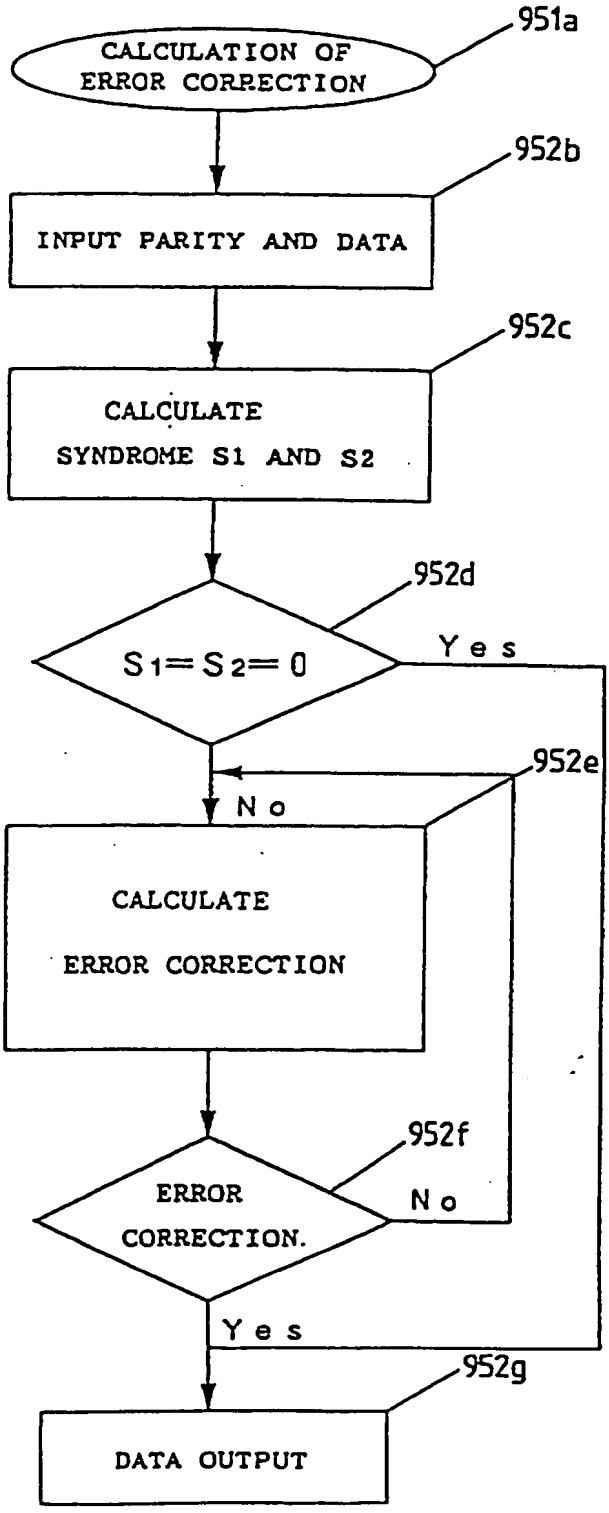

951a
CALCULATION OF ERROR CORRECTION
952b
INPUT PARITY AND DATA
952c
CALCULATE SYNDROME S1 AND S2
952d
S1=S2=0
Yes
952e
No
CALCULATE ERROR CORRECTION
952f
ERROR CORRECTION.
No
Yes
952g
DATA OUTPUT

FIG. 167

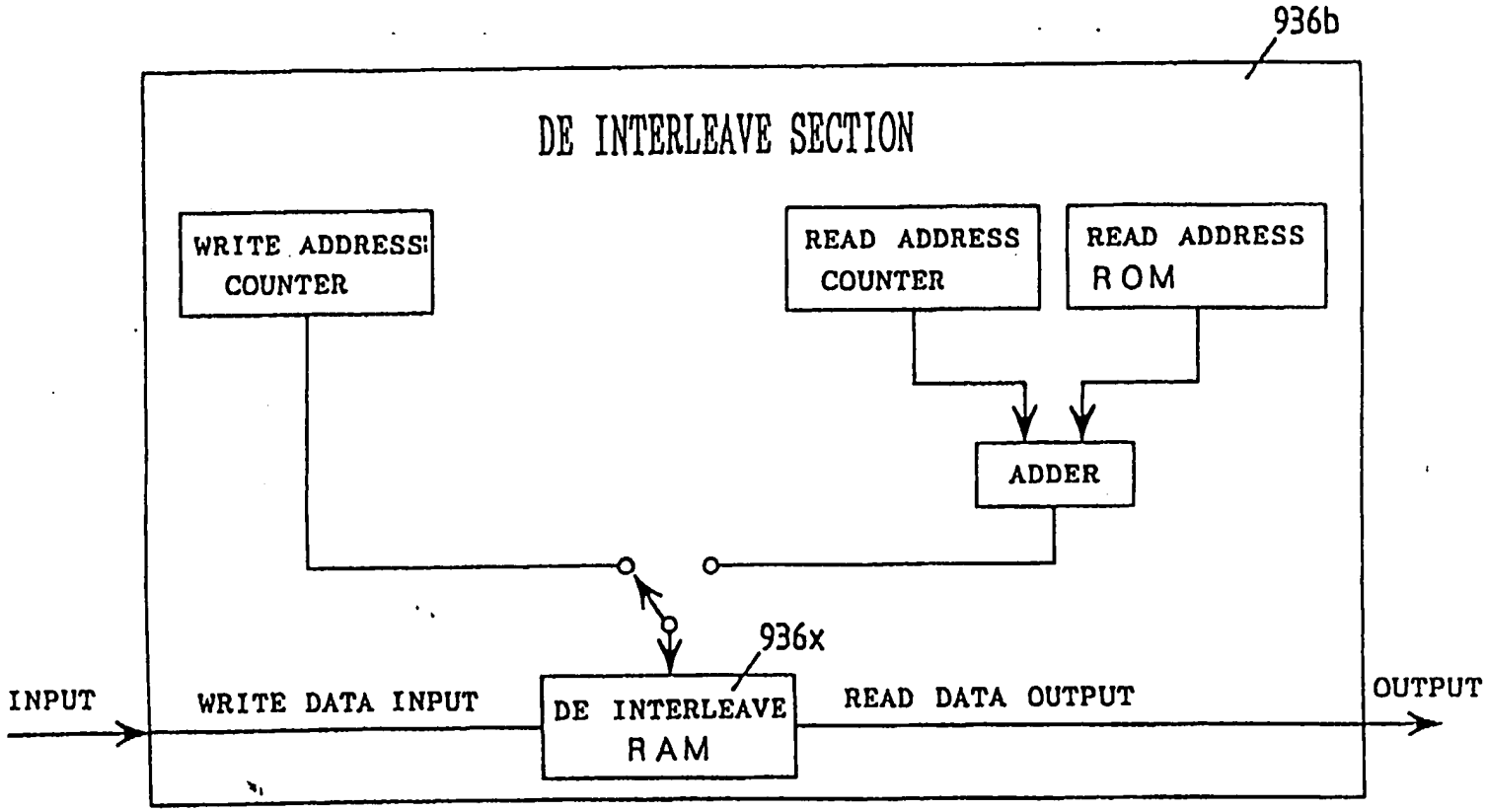

936b
DE INTERLEAVE SECTION
WRITE ADDRESS COUNTER
READ ADDRESS COUNTER
READ ADDRESS ROM
ADDER
936x
INPUT
WRITE DATA INPUT
DE INTERLEAVE RAM
READ DATA OUTPUT
OUTPUT

FIG. 168(a) Inter leave Table

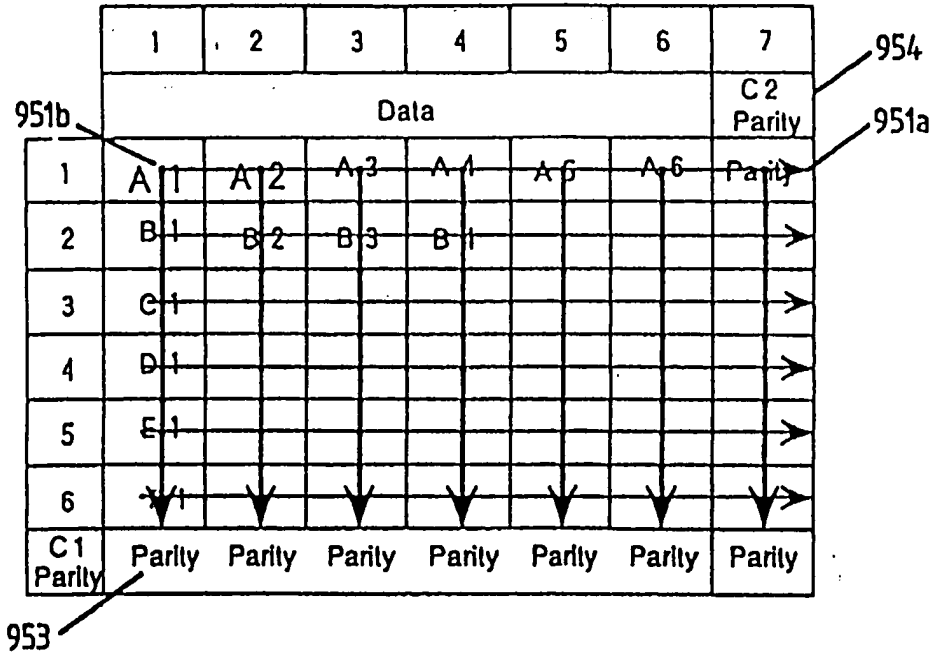


FIG. 168(b)

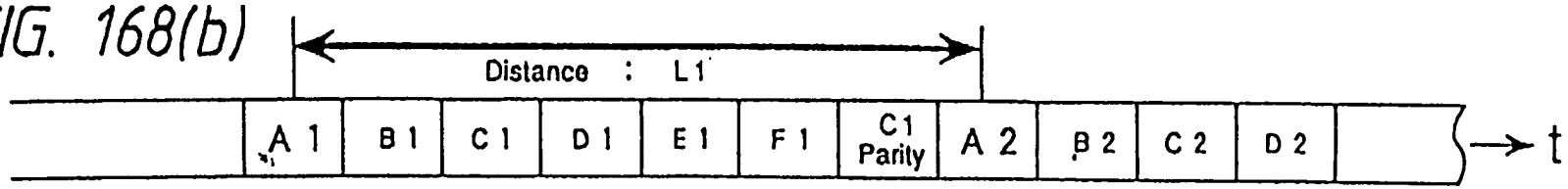


FIG. 169

Compatison of Redundancy

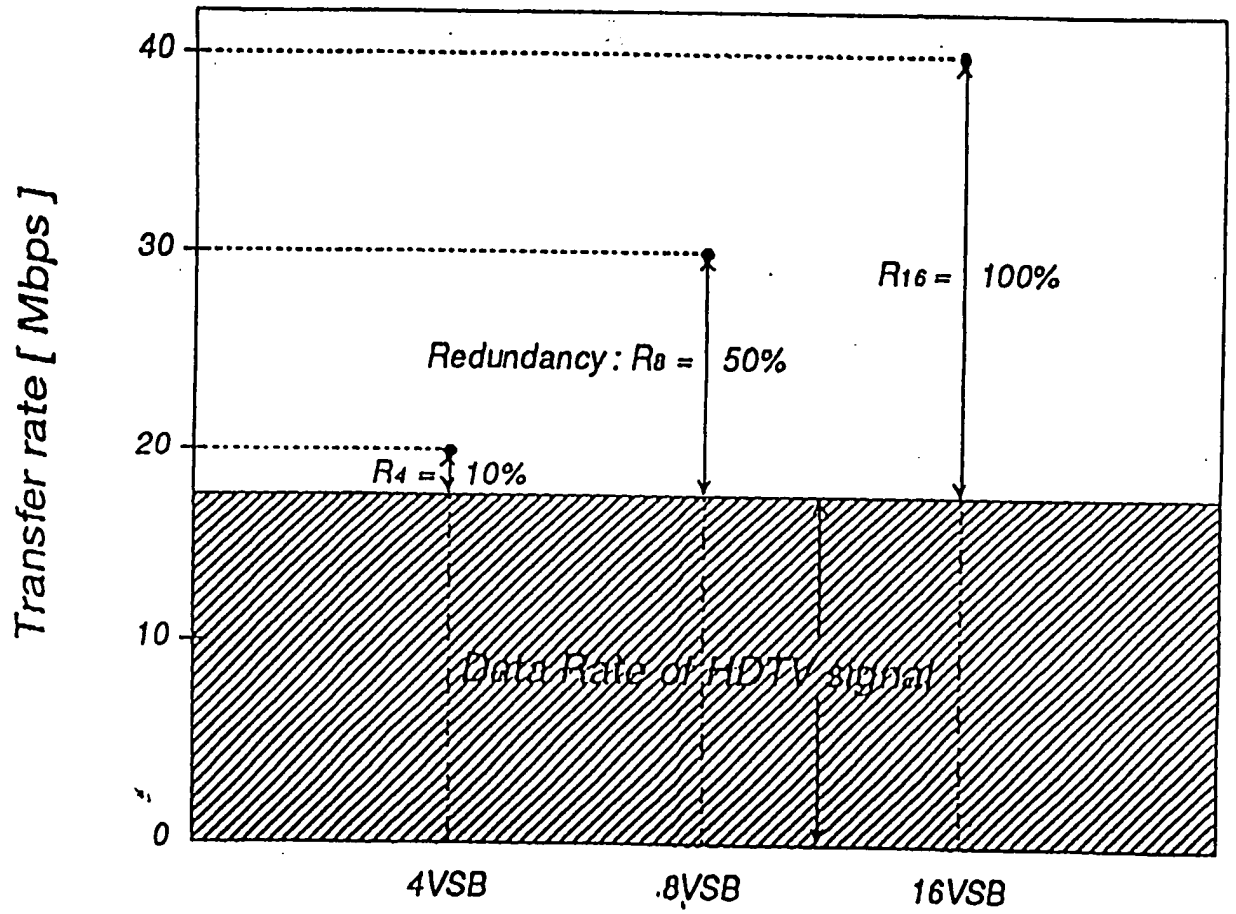


FIG. 170

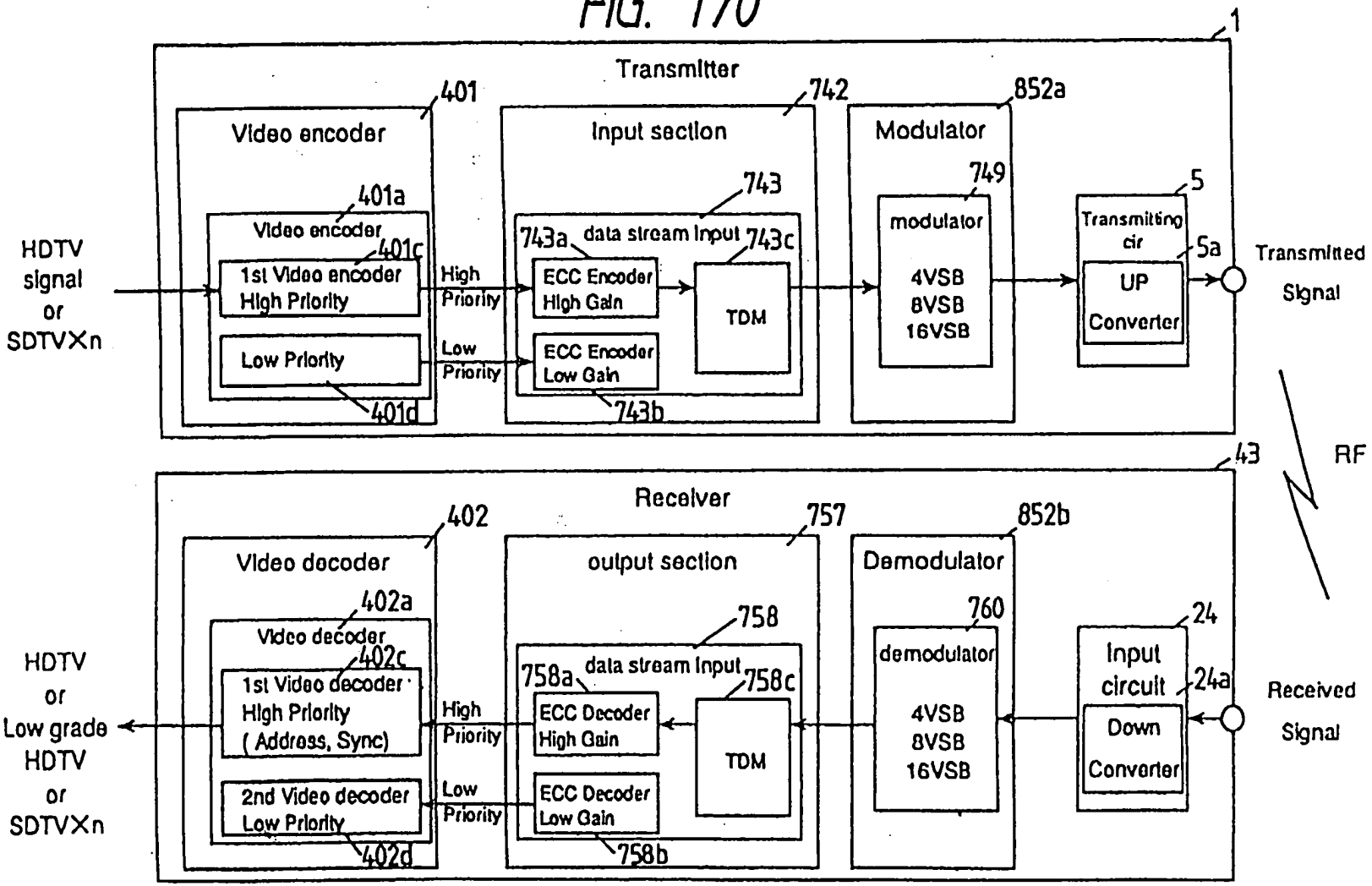

1
Transmitter
401
Video encoder
401a
Video encoder
401c
1st Video encoder
High Priority
Low Priority
401d
HDTV
signal
or
SDTVXn
High
Priority
Low
Priority
742
Input section
743
743a
data stream input
743c
ECC Encoder
High Gain
ECC Encoder
Low Gain
TDM
743b
852a
Modulator
749
modulator
4VSB
8VSB
16VSB
5
Transmitting
cir
5a
UP
Converter
Transmitted
Signal
RF
43
Receiver
402
Video decoder
402a
Video decoder
402c
1st Video decoder
High Priority
(Address, Sync)
2nd Video decoder
Low Priority
402d
HDTV
or
Low grade
HDTV
or
SDTVXn
High
Priority
Low
Priority
757
output section
758
758a
data stream input
758c
ECC Decoder
High Gain
ECC Decoder
Low Gain
TDM
758b
852b
Demodulator
760
demodulator
4VSB
8VSB
16VSB
24
Input
circuit
24a
Down
Converter
Received
Signal

FIG. 171

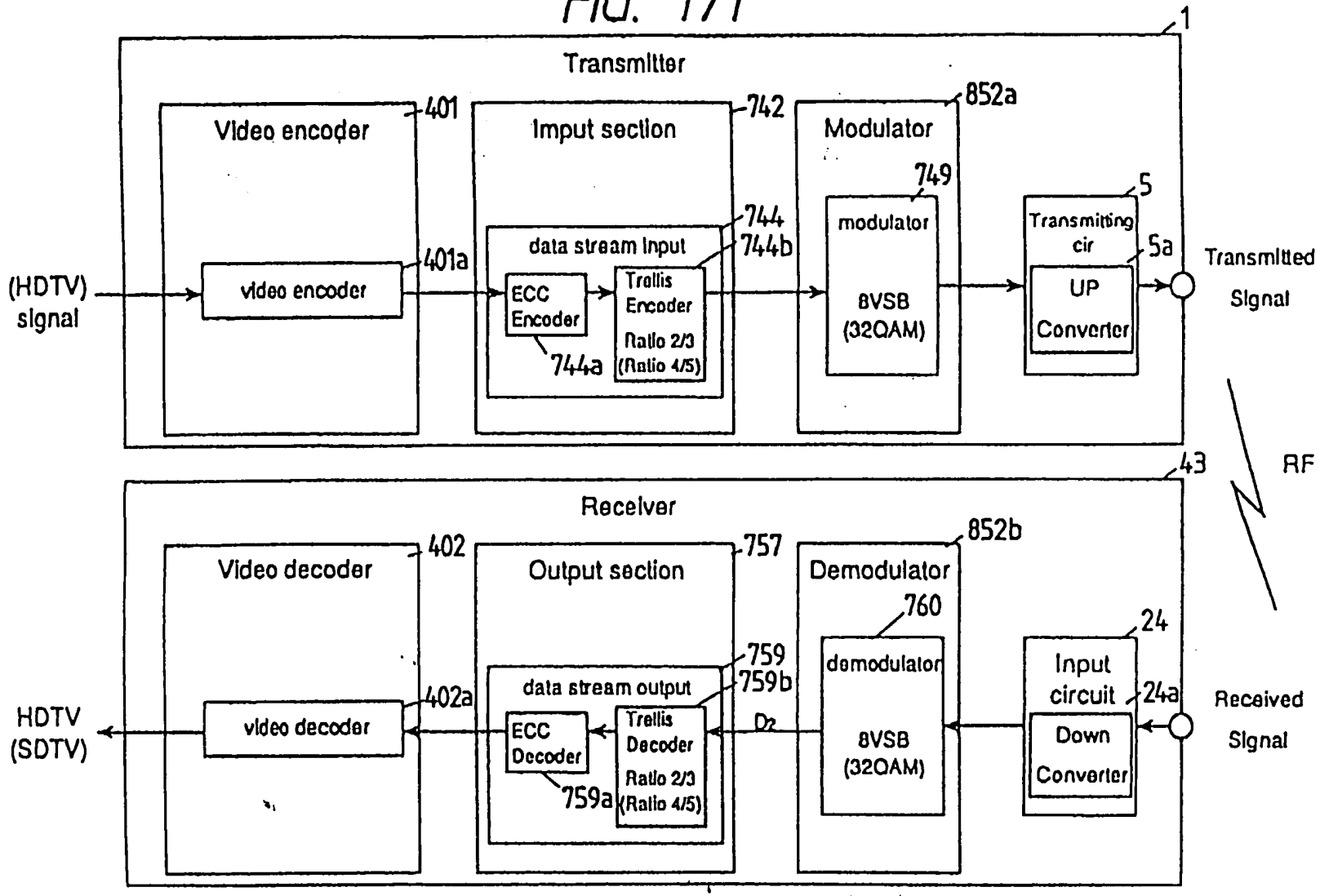

1
Transmitter
Video encoder
401
Imput section
742
Modulator
852a
749
5
744
744b
data stream input
modulator
Transmitting cir
5a
401a
(HDTV) signal
video encoder
ECC Encoder
Trellis Encoder
Ratio 2/3 (Ratio 4/5)
744a
8VSB (32QAM)
UP Converter
Transmitted Signal
RF
43
Receiver
Video decoder
402
Output section
757
Demodulator
852b
760
759
759b
data stream output
demodulator
24
Input circuit
24a
402a
HDTV (SDTV)
video decoder
ECC Decoder
Trellis Decoder
Ratio 2/3 (Ratio 4/5)
759a
D2
8VSB (32QAM)
Down Converter
Received Signal

FIG. 172

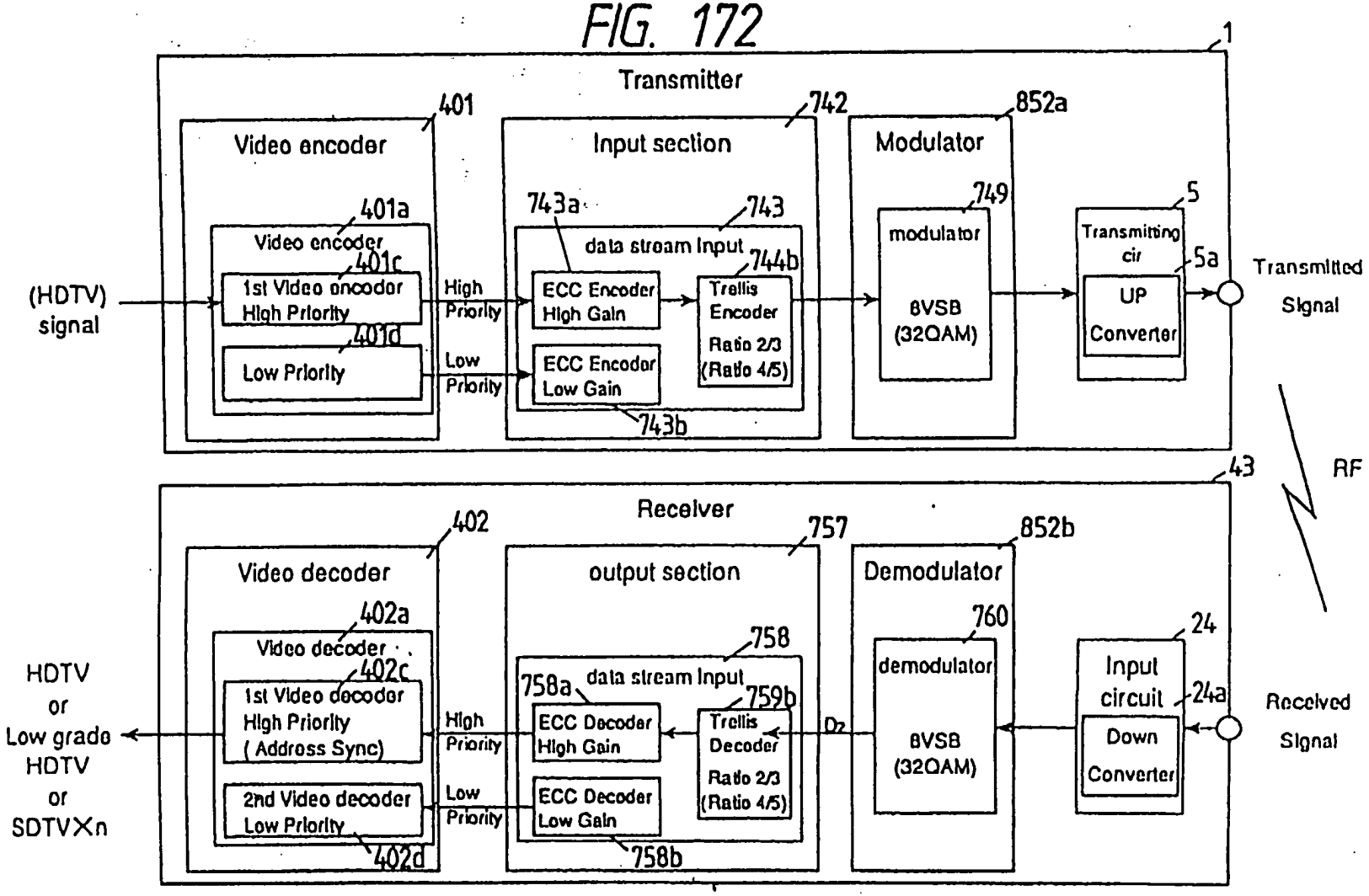
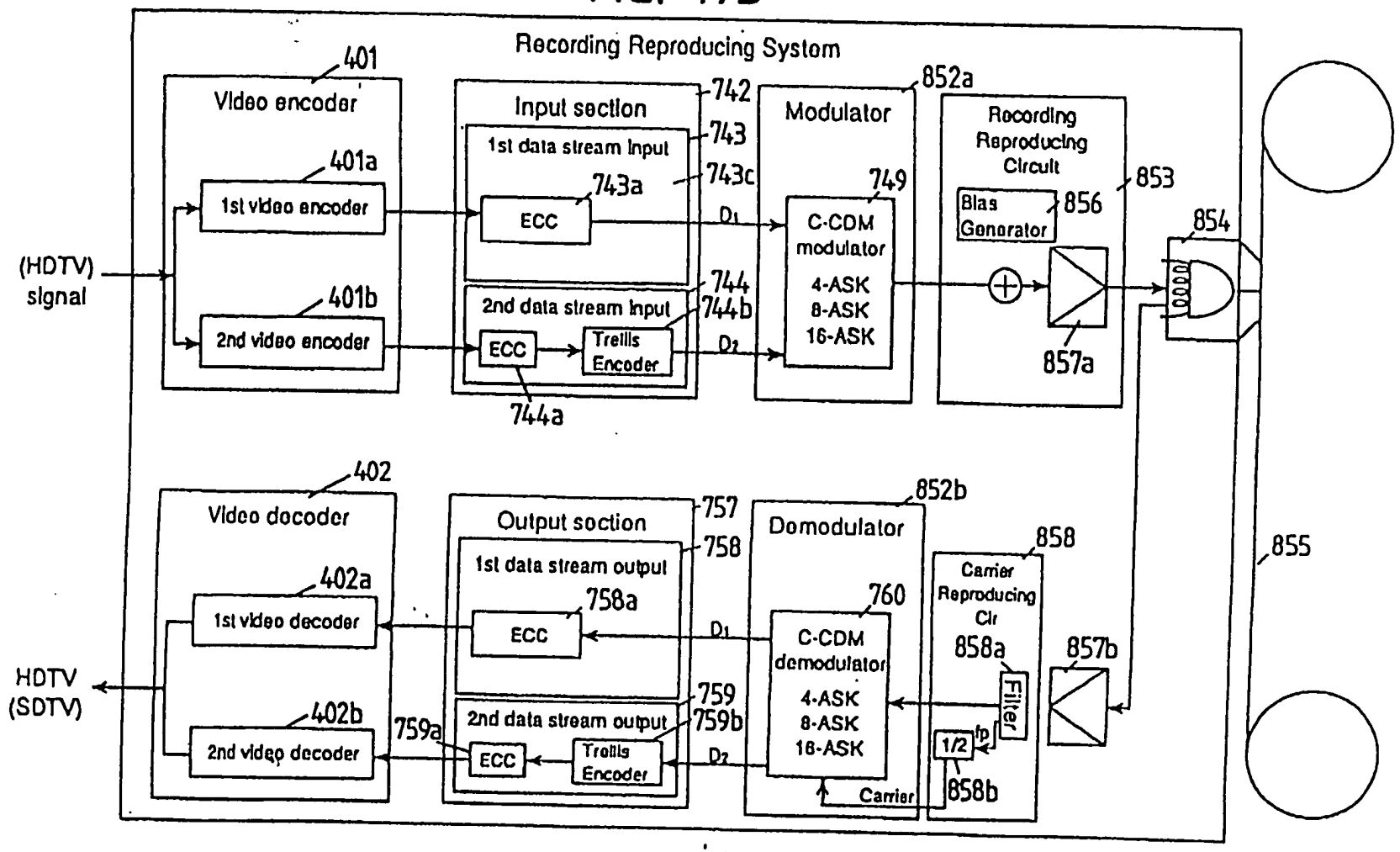

Transmitter
1
401
Video encoder
401a
Video encoder
401c
1st Video encoder
High Priority
401d
Low Priority
(HDTV)
signal
High
Priority
Low
Priority
742
Input section
743a
743
data stream Input
744b
ECC Encoder
High Gain
ECC Encoder
Low Gain
Trellis
Encoder
Ratio 2/3
(Ratio 4/5)
743b
852a
Modulator
749
modulator
8VSB
(32QAM)
5
Transmitting
cir
5a
UP
Converter
Transmitted
Signal
RF
43
Receiver
402
Video decoder
402a
Video decoder
402c
1st Video decoder
High Priority
(Address Sync)
2nd Video decoder
Low Priority
402d
HDTV
or
Low grade
HDTV
or
SDTVXn
High
Priority
Low
Priority
757
output section
758
758a
data stream Input
759b
ECC Decoder
High Gain
ECC Decoder
Low Gain
Trellis
Decoder
Ratio 2/3
(Ratio 4/5)
758b
D2
852b
Demodulator
760
demodulator
8VSB
(32QAM)
24
Input
circuit
24a
Down
Converter
Received
Signal

FIG. 173


Recording Reproducing System
401
Video encoder
401a
1st video encoder
401b
2nd video encoder
(HDTV) signal
742
Input section
743
1st data stream input
743a
ECC
743c
D1
744
2nd data stream input
744b
ECC
Trellis Encoder
D2
744a
852a
Modulator
749
C-CDM modulator
4-ASK
8-ASK
16-ASK
Recording Reproducing Circuit
853
Bias Generator
856
854
857a
855
402
Video docoder
402a
1st video decoder
402b
2nd video decoder
HDTV (SDTV)
757
Output section
758
1st data stream output
758a
ECC
759
2nd data stream output
759b
759a
ECC
Trellis Encoder
852b
Domodulator
760
C-CDM demodulator
4-ASK
8-ASK
16-ASK
Carrier
858
Carrier Reproducing Clr
858a
Filter
fp
1/2
858b
857b